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Design of Low Power 4-bit and 8-bit Shift Register in CMOS Nano Technology

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Abstract: *This research paper presents the design and analysis of low-power 4-bit and 8-bit shift registers using CMOS nanotechnology. The work focuses on four fundamental types of shift registers: Serial-In Serial-Out (SISO), Serial-In Parallel-Out (SIPO), Parallel-In Parallel-Out (PIPO), and Parallel-In Serial-Out (PISO). Initially, schematic diagrams of all configurations were designed using the DSCH tool, which also enabled the generation of timing diagrams for functional verification. The verified designs were then converted into Verilog code using DSCH's automatic code generation feature. Subsequently, the generated Verilog files were imported into the Microwind tool for simulation and physical layout design. Layouts were implemented and analyzed at three different technology nodes: 90 nm, 70 nm, and 50 nm. The primary objective was to evaluate power consumption and observe the impact of technology scaling on performance and efficiency. Power analysis was carried out for each design, demonstrating a significant reduction in power consumption as the technology node scaled down from 90 nm to 50 nm. The results indicate that nano-scale CMOS technology plays a crucial role in minimizing power dissipation while maintaining reliable performance. The proposed designs are efficient, scalable, and suitable for modern VLSI systems requiring low-power operation. This study provides a comprehensive approach to designing and analyzing shift registers, making it useful for applications in digital signal processing, communication systems, and embedded electronics*

Keywords: *CMOS Nano Technology, Shift Register, Low Power Design, SISO, SIPO, PIPO, PISO, DSCH, Microwind, Verilog.*

1. Introduction

In modern digital systems, shift registers play a vital role in data storage, data transfer, and sequential logic operations. They are widely used in applications such as digital signal processing, communication systems, microprocessors, and embedded systems. A shift register is essentially a chain of flip-flops connected in such a way that data can be shifted in a serial or parallel manner depending on the configuration. With the rapid advancement in Very Large Scale Integration (VLSI) technology, there is a growing demand for efficient, high-speed, and low-power circuit designs, especially as devices become more compact and portable.

The continuous scaling of CMOS technology into nanometer regimes has significantly improved the performance of digital circuits. However, this scaling also introduces several challenges, particularly in terms of power consumption, leakage currents, and reliability. As technology nodes shrink from 90 nm to 40 nm and further down to 25 nm, dynamic and static power dissipation becomes a critical concern [1, 2]. Therefore, designing low-power shift registers is essential for enhancing battery life and overall system efficiency in modern electronic devices.
Shift registers are generally classified into four main types based on their mode of operation: SISO, SIPO, PIPO, and PISO. Each configuration serves a specific purpose. For example, SISO is mainly used for data delay, SIPO is used for serial-to-parallel data conversion, PISO for parallel-to-serial conversion, and PIPO for temporary data storage. The

flexibility and versatility of these configurations make shift registers an integral component in digital circuit design [3].

In this research work, both 4-bit and 8-bit shift registers have been designed and analyzed using CMOS nano-technology. The design process begins with schematic creation using the DSCH tool, which provides a user-friendly environment for digital circuit design and verification. DSCH allows designers to create logic circuits using basic components such as flip-flops, logic gates, and interconnections. Additionally, it enables the generation of timing diagrams, which are essential for verifying the functional correctness of sequential circuits [4].

Once the schematic design and timing verification are completed, the DSCH tool is used to automatically generate the corresponding Verilog code. Verilog is a widely used HDL that facilitates the modeling and simulation of digital systems. The generated Verilog code ensures that the logical behavior of the shift register is accurately represented and can be further used for physical design implementation [5].

The next stage involves importing the Verilog code into the Microwind tool for simulation and layout design. Microwind is a powerful VLSI design tool that enables designers to create and simulate integrated circuit layouts at various technology nodes. In this work, layouts have been developed for 90 nm, 40 nm, and 25 nm technologies to analyze the impact of scaling on circuit performance. The layout design includes transistor placement, routing, and optimization to achieve efficient area utilization and minimal power consumption [6, 7].

Power analysis is a crucial aspect of this study, as low power consumption is a primary objective. By simulating the designs at different technology nodes, it becomes possible to evaluate how scaling affects power dissipation. Typically, as the technology node decreases, the supply voltage also reduces, leading to lower dynamic power consumption. However, leakage power may increase due to short-channel effects, which must be carefully managed during the design process [8].

Overall, this research focuses on designing efficient 4-bit and 8-bit shift registers using various configurations and analyzing their performance across multiple CMOS technology nodes. The study highlights the importance of low-power design techniques in nanoscale VLSI systems and demonstrates how tools like DSCH and Microwind can be effectively used for schematic design, simulation, and layout implementation. The outcomes of this work are highly relevant for the development of energy-efficient digital systems in modern electronics [9].

2. Shift Register

A shift register is a type of sequential digital circuit used to store and transfer binary data. It is made up of a series of flip-flops (usually D flip-flops) connected in such a way that the output of one flip-flop becomes the input of the next. This arrangement allows data to “shift” from one stage to another with each clock pulse.

In a shift register, data can be entered either serially (one bit at a time) or in parallel (multiple bits at once), depending on the configuration. Similarly, the output can also be taken in serial or parallel form. Based on these input-output combinations, shift registers are classified into four main types: SISO, SIPO, PIPO, and PISO. Each type serves different purposes in digital systems, such as data storage, data conversion, and data transfer.

The operation of a shift register is controlled by a clock signal. On every clock pulse, the data stored in each flip-flop moves one position to the next flip-flop in the chain. This shifting action enables temporary data storage and sequential data processing. Additional control signals like reset or clear are often used to initialize the register to a known state [10, 11].

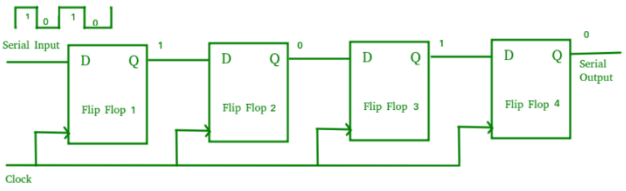

Fig. 1: SISO

Shift registers are widely used in applications such as digital communication systems, signal processing, counters, and memory devices. They play an important role in converting data formats (serial to parallel and vice versa), delaying signals, and synchronizing data flow in digital circuits.

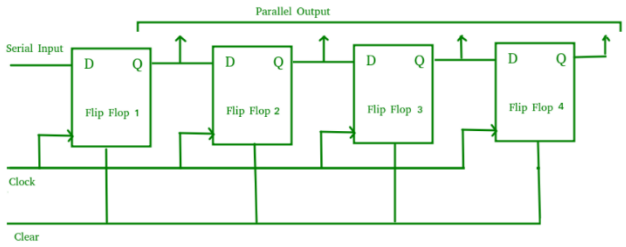

Fig. 2: SIPO

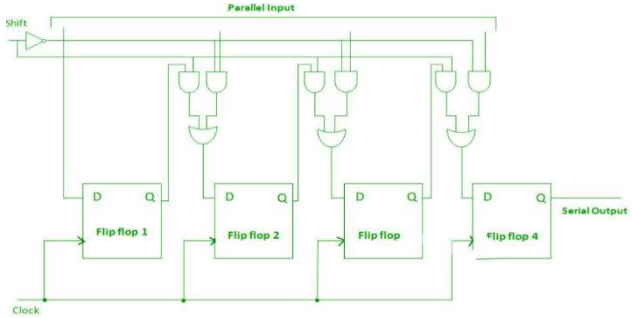

Fig. 3: PISO

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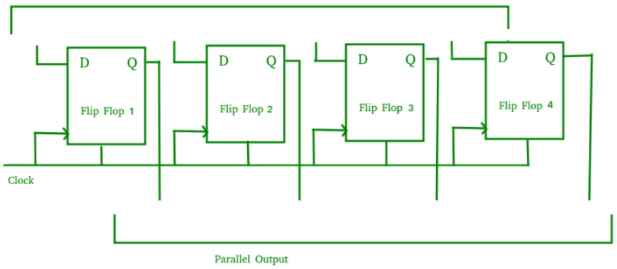

Fig. 4: PIPO

3. Layout And Timing Diagram

3.1 Tool:

DSCH (Digital Schematic Editor) is a user-friendly tool used for designing and simulating digital circuits at the schematic level. It allows designers to create circuits using logic gates and flip-flops, generate timing diagrams, and verify functional behavior. One of its key features is the automatic generation of Verilog code, which helps in bridging the gap between logical design and hardware description.

Microwind is a VLSI design tool used for physical layout design and simulation of integrated circuits. It enables designers to implement CMOS layouts, perform real-time simulations, and analyze parameters such as power consumption and area at different technology nodes (e.g., 90 nm, 40 nm, 25 nm). Together, DSCH and Microwind provide a complete design flow from schematic design to layout implementation in VLSI systems.

3.2 Result

The given fig. 5 & Fig. 6 represents a 4-bit & 8-bit shift register implemented using a chain of D flip-flops in a sequential circuit. Each block labeled “dreg” corresponds to a D-type flip-flop, and they are connected in series to form the shift register structure. The input labeled “Data in” is applied to the first flip-flop, and with every clock pulse, the data is shifted from one flip-flop to the next. This sequential shifting process allows the circuit to store and transfer data bit by bit across the register stages.

A common clock signal is connected to all flip-flops, ensuring synchronized operation. On each active clock edge, the data present at the input of each flip-flop is transferred to its output. The output of one flip-flop becomes the input of the next, which creates the shifting effect. The outputs labeled (out1, out2, out3, out4) represent the state of each stage, showing how the input data propagates through the register over time. This behavior is typically associated with a Serial-In Serial-Out (SISO) or Serial-In Parallel-Out (SIPO) configuration, depending on how outputs are used.

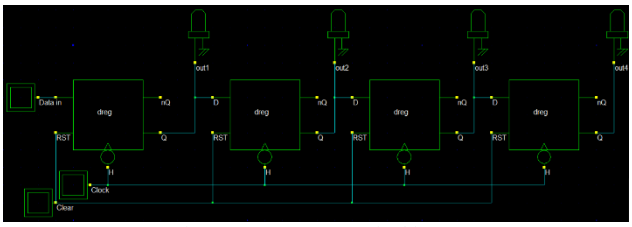

Fig. 5: DSCH Layout of 4-bit SIPO

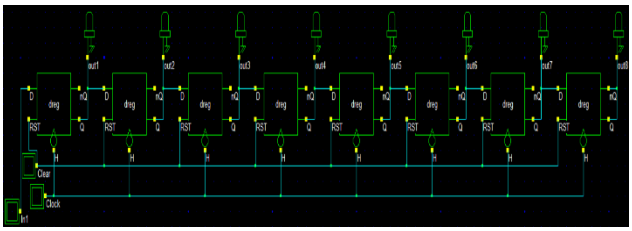

Fig. 6: DSCH Layout of 8-bit SIPO

Additionally, control signals such as reset (RST) and clear are included to initialize the flip-flops to a known state, usually logic ‘0’. This ensures proper operation during the start of the circuit. The diagram clearly demonstrates how sequential logic elements are used to implement data storage and controlled data movement, which is essential in digital systems such as communication interfaces, buffering, and data processing applications.

The output result of the designed 4-bit and 8-bit shift registers are illustrated in Fig. 7 and Fig. 8, respectively.

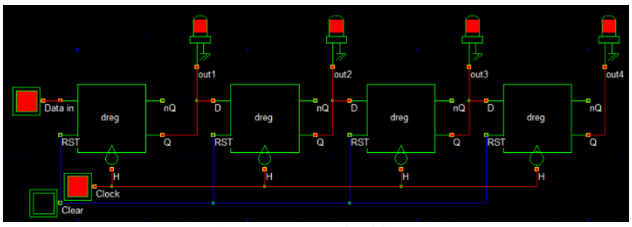

Fig. 7: Output of 4-bit SIPO

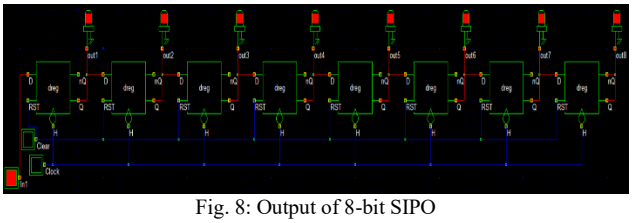

Fig. 8: Output of 8-bit SIPO

These figures demonstrate the correct shifting operation of input data across each flip-flop stage with every clock pulse. It can be observed that the input data propagates sequentially through the register, validating the proper functioning of the designed SISO, SIPO, PIPO, and PISO configurations.

Furthermore, the corresponding timing diagrams are presented in Fig. 9 and Fig. 10, which clearly show the

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synchronization between the clock signal and the output transitions. The timing analysis confirms that data shifting occurs precisely at the triggering edge of the clock, ensuring reliable sequential operation. These results verify the accuracy and stability of the proposed shift register designs.

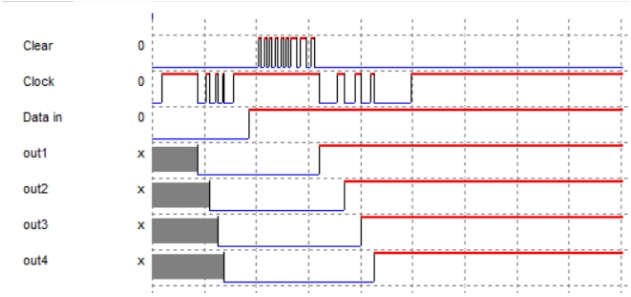

Fig. 9: Timing Diagram of 4-bit SIPO

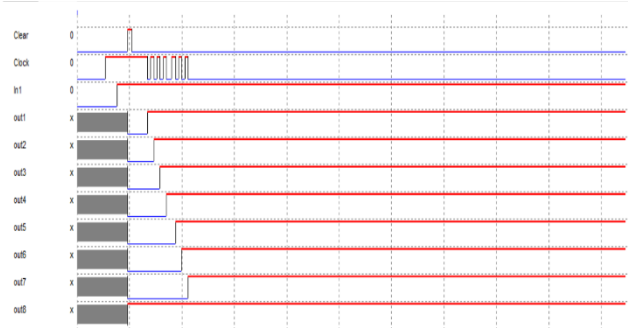

Fig. 10: Timing Diagram of 8-bit SIPO

The given Fig. 11 to Fig. 14 represents a 4-bit & 8-bit PIPO shift register implemented using D flip-flops. In this circuit, four D flip-flops (labeled as "dreg") are connected in parallel, meaning that each flip-flop receives its own independent input (in1, in2, in3, in4). Unlike serial shift registers, there is no data shifting between stages; instead, all bits are loaded simultaneously.

A common clock signal is connected to all flip-flops, ensuring synchronized operation. When the clock pulse is applied, all input bits (in1 to in4) are captured at the same time and stored in their respective flip-flops. The outputs (out1, out2, out3, out4) reflect these stored values simultaneously after the clock edge. This parallel loading and parallel output make the PIPO register very fast compared to serial configurations.

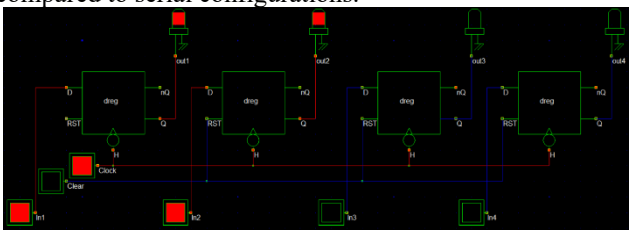

Fig. 11: Output of 4-bit PIPO

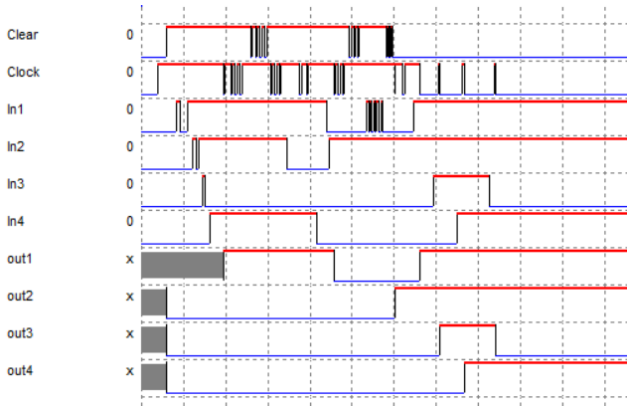

Fig. 12: Timing Diagram of 4-bit PIPO

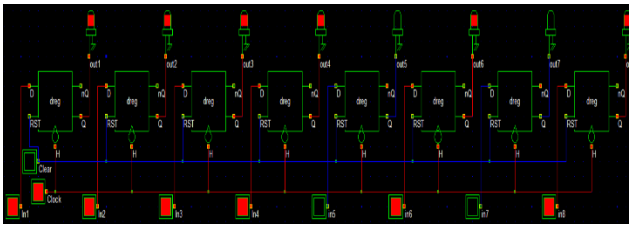

Fig. 13: Output of 8-bit PIPO

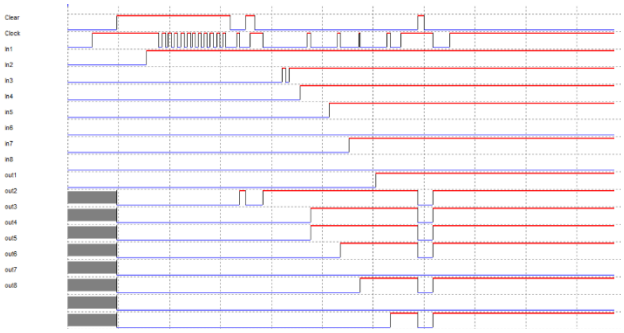

Fig. 14: Timing Diagram of 4-bit PIPO

The given fig. 15 and fig. 16 represents a 4-bit SISO shift register implemented using a chain of D flip-flops. In this configuration, the data is applied serially through a single input labeled In1, and it passes through each flip-flop one stage at a time.

Each block labeled "dreg" is a D flip-flop, and they are connected in series such that the output (Q) of one flip-flop is connected to the input (D) of the next. A common clock signal is provided to all flip-flops, ensuring synchronized operation. On every active clock edge, the input data shifts from the first flip-flop to the second, then to the third, and finally to the fourth. This step-by-step movement of data is the fundamental operation of a shift register.

The final output is taken from the last flip-flop, labeled out4, which represents the serial output of the register. This means that after four clock pulses, the input data bit applied at In1 will appear at the output. The intermediate outputs

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(nQ or Q of each stage) indicate how the data propagates through each stage over time.

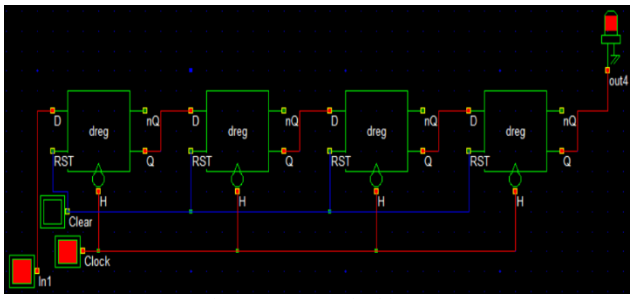

Fig. 15: Output of 4-bit SISO

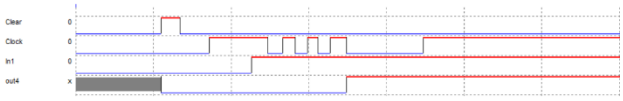

Fig. 16: Timing Diagram of 4-bit SISO

The given fig. 17 and fig. 18 represents a 4-bit PISO shift register implemented using D flip-flops along with combinational logic (AND and OR gates). This design allows data to be loaded in parallel and then shifted out serially, making it useful for parallel-to-serial data conversion in digital communication systems.

In this circuit, the inputs in1, in2, in3, and in4 represent the parallel data inputs applied simultaneously to the register. A control signal labeled Shift determines the mode of operation. When the Shift signal is inactive (logic 0), the circuit operates in parallel load mode, where all input bits are loaded into their respective flip-flops at the same time during a clock pulse. This is achieved through the combinational logic (AND-OR network), which selects the parallel inputs.

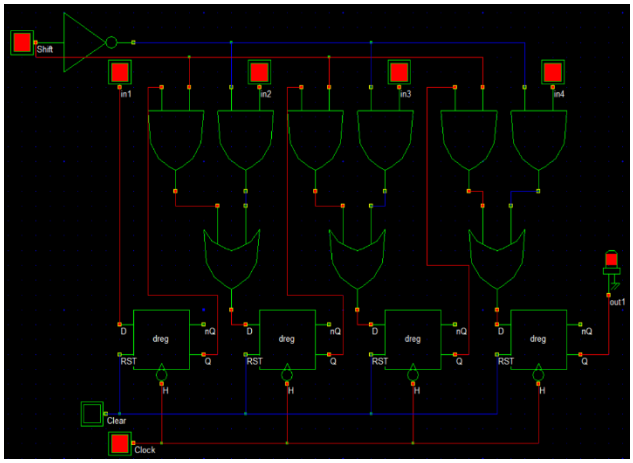

Fig. 17: Output of 8-bit PISO

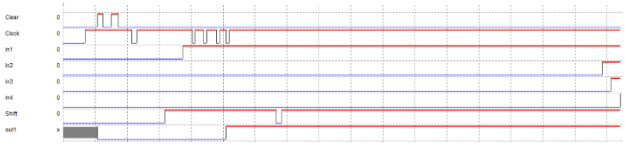

Fig. 18: Timing Diagram of 4-bit PISO

When the Shift signal is active (logic 1), the circuit switches to shift mode. In this mode, the data stored in the flip-flops is shifted sequentially from one stage to the next with each clock pulse. The output of each flip-flop is routed to the next stage through the logic gates, enabling serial data movement. The final output is taken from the last flip-flop, labeled out1, which provides the serial output of the register.

A common clock signal synchronizes all flip-flops, ensuring that data loading and shifting occur at precise intervals. The Clear and RST (reset) signals are used to initialize the register to a known state (usually logic 0), ensuring reliable operation at the start.

4. Power Dissipation

Power dissipation in Microwind is calculated through built-in simulation tools that analyze the switching activity of the designed CMOS circuit. After completing the layout design, the circuit is simulated using real-time logic transitions. Microwind computes power based on both dynamic power and static (leakage) power components.

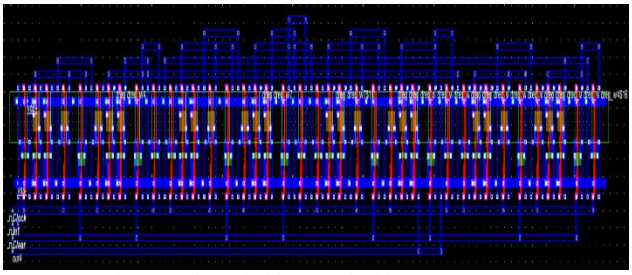
Fig. 19: Microwind layout of 4-bit SISO at 90 nm

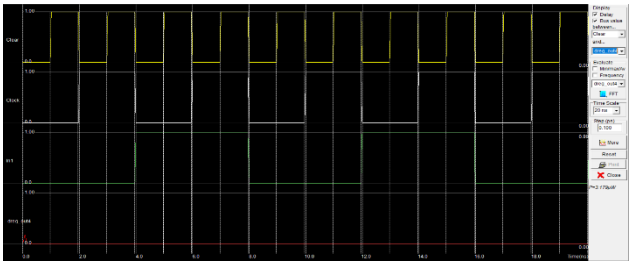
Fig. 20: Power Dissipation of 4-bit SISO at 90 nm

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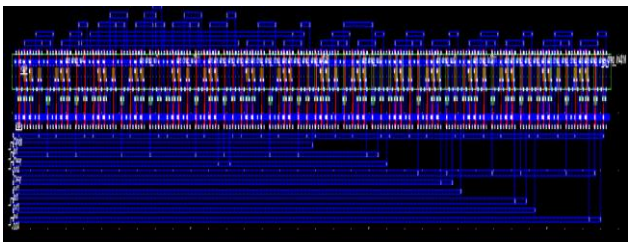

Fig. 21: Microwind layout of 4-bit PIPO at 90 nm

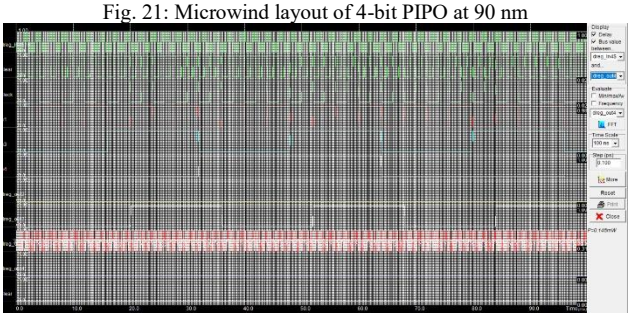

Fig. 22: Power Dissipation of 4-bit PIPO at 90 nm

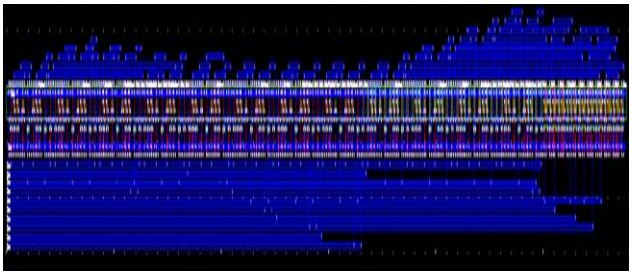

Fig. 23: Microwind layout of 4-bit PISO at 90 nm

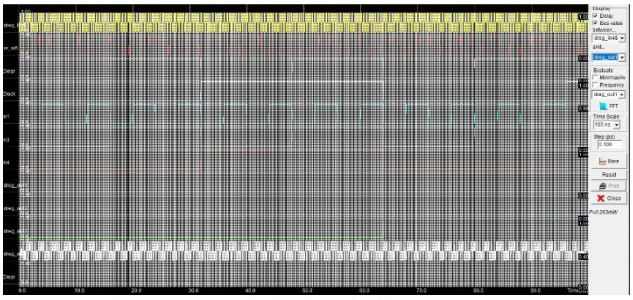

Fig. 24: Power Dissipation of 4-bit PISO at 90 nm

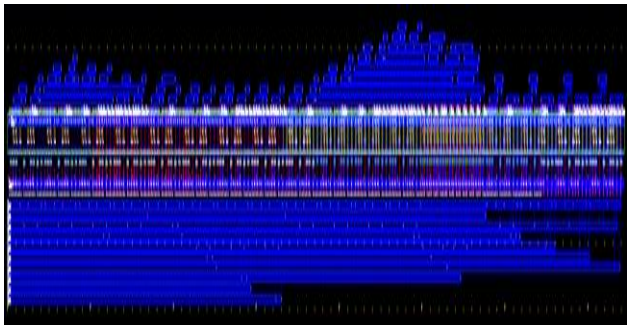

Fig. 25: Microwind layout of 4-bit SIPO at 90 nm

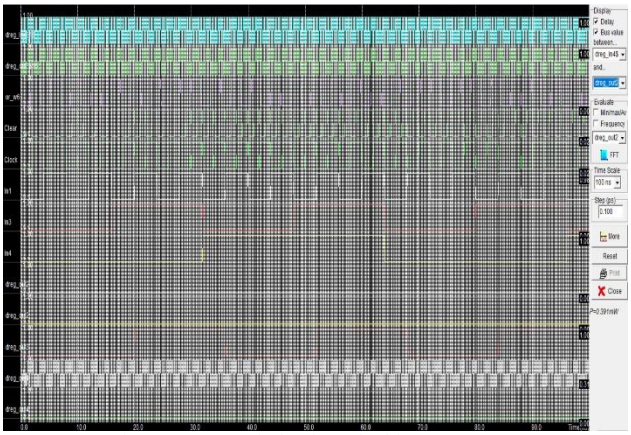

Fig. 26: Power Dissipation of 4-bit SIPO at 90 nm

5. Conclusion

This research work successfully presents the design and analysis of low-power 4-bit and 8-bit shift registers using CMOS nano-technology. All four major configurations—SISO, SIPO, PIPO, and PISO—were implemented and verified to demonstrate their functional correctness and practical applicability in digital systems. The use of the DSCH tool enabled efficient schematic design and timing verification, ensuring accurate sequential operation of the circuits. Furthermore, the automatic generation of Verilog code simplified the transition from logical design to physical implementation.

The generated Verilog designs were successfully imported into the Microwind tool, where detailed layout designs were created and simulated. The layouts were implemented across three different technology nodes: 90 nm, 70 nm, and 50 nm, allowing a comprehensive analysis of technology scaling effects. The study clearly shows that as the technology scales down, there is a significant reduction in overall power consumption, making nanoscale CMOS technology highly suitable for low-power VLSI applications.

Power analysis results confirm that optimized shift register designs can effectively minimize energy dissipation while maintaining reliable performance. Although leakage power becomes more prominent at lower technology nodes, the overall benefits of reduced dynamic power dominate, leading to improved efficiency. The proposed designs are compact, scalable, and suitable for integration into modern digital systems such as communication devices, signal processing units, and embedded applications.

In conclusion, this work demonstrates a complete design flow from schematic to layout using industry-relevant tools and highlights the importance of low-power design in nanoscale CMOS technology. The findings contribute to the development of energy-efficient digital circuits and provide a strong foundation for future research in advanced VLSI system design.

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