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# Harmonic and Stress Reduction in a DC-DC Converter Using a Five-Level Inverter

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***Abstract***: *This study presents a novel single-phase five-level Current Source Inverter (CSI) topology designed to enhance harmonic and stress reduction in DC-DC converters. The proposed CSI utilizes eight switches and two DC link inductors to generate five distinct current levels, ensuring even current distribution and a symmetrical structure. Notably, it can also operate in single-inductor mode, although this results in increased inductor current ripple. The study provides a detailed analysis of the inverter's functional operation, including switching states and conduction paths, and introduces an effective algorithm for balancing inductor currents, validated through both theoretical and experimental approaches. The H-Bridge (HB) submodule allows for output current polarity reversal, with HB switches operating at a low fundamental frequency and non-HB switches at a higher carrier frequency, optimizing switching loss and switch ratings. Simulation and experimental results confirmed a voltage boost ratio of 1:4 and demonstrated the inverter's capability in harmonic reduction and stress minimization. Future work will explore closed-loop operation, loss modeling, and advanced modulation techniques.*

***Keywords:*** *Current Source Inverter (CSI), Five-Level Inverter, Harmonic Reduction, Inductor Current Balancing, Voltage Boosting*

## 1. Introduction

In modern power electronics, the quest for improving efficiency and performance in DC-DC converters has led to the development of advanced inverter topologies. One such innovation is the five-level Current Source Inverter (CSI), which offers a promising solution for harmonic and stress reduction in DC-DC converters. Unlike traditional inverters that may exhibit higher harmonic distortion and stress on components, a five-level CSI introduces multiple voltage levels, significantly reducing harmonic content and smoothing the output current. By employing eight switches and two DC link inductors, this topology enables the generation of five distinct current levels, enhancing the converter's overall performance and reliability. The five-level CSI's ability to operate in both dual-inductor and single-inductor modes adds versatility, although single-inductor operation results in increased current ripple. The symmetrical structure of the proposed inverter ensures balanced current distribution between inductors, mitigating harmonic issues and reducing stress on components. Detailed analysis and practical implementation demonstrate that this innovative design not only minimizes switching losses but also optimizes component ratings. This paper explores the effectiveness of the five-level CSI in reducing harmonics and stress, presenting theoretical, simulation, and experimental insights into its operation and performance.

## 2. Methodology

Figure 1 illustrates the schematic of the proposed current-source inverter, which comprises two inductors and eight reverse-blocking switches. Each switch is implemented with a transistor-diode pair in series. Switches S12, S13, S22, and S23 function as H-Bridge (HB) converters, reversing the output current at each fundamental half-cycle.

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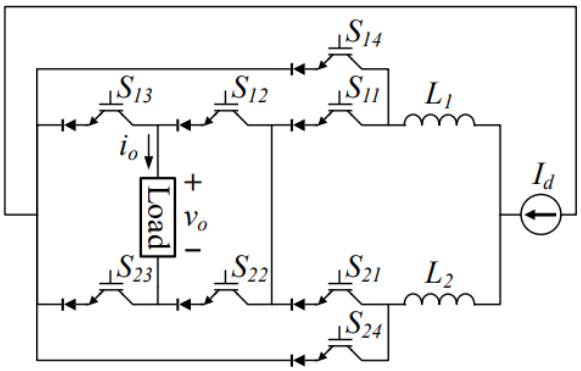



Figure 1 Schematic of the proposed single-phase five-level current-source inverter

**Inverter Switching States**

Table 1 outlines the practical switching states of the proposed inverter, and Figure 2 illustrates the corresponding conduction paths. Throughout this section, an ideal DC current source with a magnitude of Id is assumed. For simplicity, the inductor currents iL1 and iL2 are considered to each carry half of the source current, Id/2.

**Table 1 Switch states for the various output current levels**

| $S_{11}$ | $S_{12}$ | $S_{13}$ | $S_{14}$ | $S_{21}$ | $S_{22}$ | $S_{23}$ | $S_{24}$ | $V_{L1} - V_{L2}$ |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 $I_d$ |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | $-v_o$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | $+v_o$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | $-v_o$ $-I$ $d/2$ |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $+v_o$ |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 $-I_d$ |

Figure 2a shows the conduction path of the inverter output current Id, where switches S11 and S21 each carry half of the source current. These currents merge, are delivered to the load, and then return to the source through switches S12 and S23. Figure 2b illustrates one of the two possible conduction paths for the output current Id/2. In this state, inductor current IL1 flows to the load via switches S11 and S12 and returns to the source through S23, while inductor current IL2 is directly fed back to the source via S24. Another switching state delivering Id/2 to the load is depicted in Figure 2c. Here, inductor current IL2 is routed to the load and back to the source through switches S21, S12, and S23, while inductor current IL1 is directly returned to the source through S14. These switching states correspond to the positive current half-cycle, with HB switches S12 and S23 remaining on continuously.

Figure 2d illustrates the zero-current state, where inductor currents IL1 and IL2 return to the source through switches S14 and S24, respectively. It is important to note that this zero-current state is independent of the state of HB switches S12, S13, S22, and S23, which can be adjusted based on practical considerations.

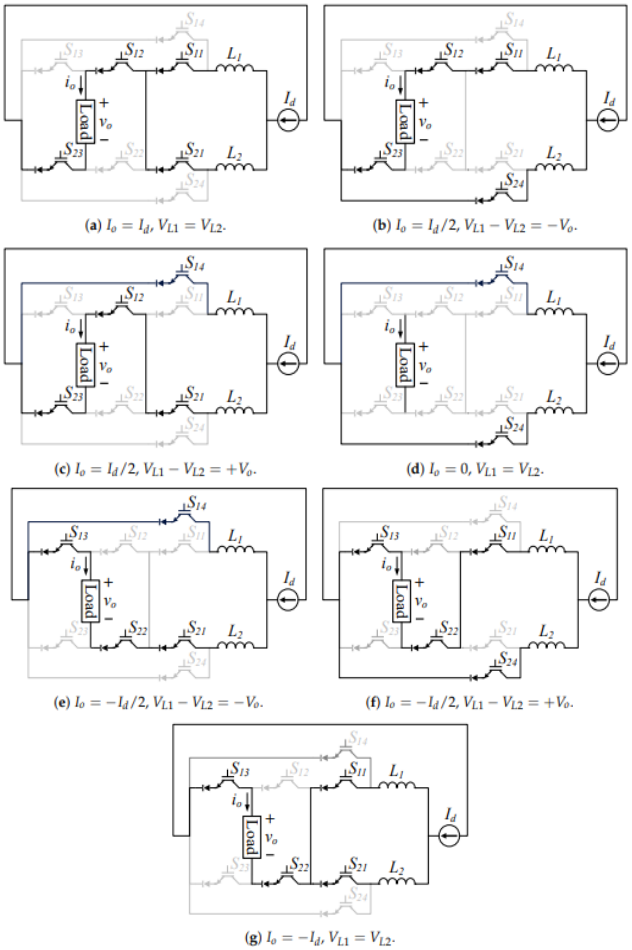



Figure 2 Conduction paths for the various output current levels

The switching states for the negative current half-cycle are depicted in Figures 2e–g. To reverse the inverter output current, the HB switches are toggled, turning off switches $S_{12}$ and $S_{23}$ and turning on switches $S_{13}$ and $S_{22}$ continuously. Similar to the positive current half-cycle, the output current of −Id/2 can be achieved using two different switching states. The first state is shown in Figure 2e, where inductor current IL2 flows through switches $S_{21}$ and $S_{22}$ to the load and returns to the source via $S_{13}$. Meanwhile, inductor current IL1 is directly fed back to the source through $S_{14}$. Another way to achieve −Id/2 is by turning on switches $S_{11}$, $S_{22}$, and $S_{13}$, as shown in Figure 2f. In this configuration, inductor current IL1 returns to the source via $S_{24}$.

Finally, the output current of −Id is realized through the conduction path shown in Figure 2g. Similar to the positive case, inductor currents IL1 and IL2 flow through switches $S_{11}$ and $S_{21}$, merge, and are routed to the load via $S_{22}$, then return to the source through $S_{13}$. The above analysis applies to binary inverter operation, where a current of the same magnitude, Id/2, flows through inductors IL1 and IL2. By asymmetrically dividing the source current between the inductors to achieve a trinary current ratio of IL1 : IL2 = 1 : 3, a seven-level current source inverter (CSI) is derived. This can be inferred by offsetting the inductor currents accordingly and following the analysis provided in this section. However, the means of current offsetting and its impact on the inverter's operation are beyond the scope of this paper.

**Inductor Current Balancing**

For normal inverter operation, the inductor currents must remain balanced within a fundamental cycle. This balance is maintained by selectively employing the redundant switching states for output currents io = ± Id/2, as depicted in Figure 2. According to Kirchhoff's current law, we have:

$$i_{L1} + i_{L2} = I_d \quad (1)$$

for all switching states illustrated in Figure 2. Applying Kirchhoff's voltage law to Figure 2b,e yields

$$v_{L1} - v_{L2} = -v_o \quad (2)$$

which results in

$$L_1\frac{di_{L_1}}{dt} - L_2\frac{di_{L_2}}{dt} = -v_o \quad (3)$$

Substituting (1) into (3), the following equation can be derived:

$$\frac{di_{L_1}}{dt} = -\frac{v_o}{L_1 + L_2} \quad (4)$$

Similarly, applying the above analysis to Figure 2c,f, we get

$$\frac{di_{L_1}}{dt} = +\frac{v_o}{L_1 + L_2} \quad (5)$$

Based on (4) and (5), the following rule for the balancing of inductor currents can be derived:

$$S_{11} = S_{24} = \frac{1 + sgn(i_o)sgn(v_o)sgn(i_{L_1} - i_{L_2})}{2}, \quad \{i_o = \quad (6)$$

where sgn() denotes the sign function:

$$sgn(x) = \begin{cases} +1 & x \geqslant 0 \\ -1 & x < 0 \end{cases} \quad (7)$$

and $S_{11} = S_{24} = S_{21} = S_{14}$ for inverter output currents $\pm I_d/2$.

HB switches are determined according to the output current polarity as follows:

$$S_{12} = S_{23} = \frac{1 + sgn(i_o)}{2} \quad (8)$$

while S13 = S22 = S12 = S23 regardless of the output current.

It is important to note that the above analysis can be adapted for single-inductor operation of the inverter. In this mode, one inductor is replaced by a short circuit, and the current in the remaining inductor is balanced to half the source current. Current balancing in single-inductor operation follows a similar approach to the dual-inductor operation described earlier. For intermediate current levels of io = ±Id/2, the instantaneous load voltage can be applied to the single inductor in either polarity by selecting the appropriate redundant switching states. Consequently, equations (4) and (5) are simplified to:

$$\frac{di_{L_1}}{dt} = \pm\frac{v_o}{L_1} \quad (9)$$

where the positive and negative signs correspond to, respectively, Figure 2b,e and Figure 2c,f. The resulting balancing rule then becomes

$$S_{11} = S_{24} = \frac{1 + sgn(i_o)sgn(v_o)sgn(i_{L_1} - i_s/2)}{2}, \quad \left\{i_o = \pm\frac{I_d}{2}\right\} \quad (10)$$

where $i_s$ is the instantaneous current supplied by the source. It should be noted that in this scenario, the single inductor will experience a voltage drop equal to the full magnitude of the instantaneous load voltage. Consequently, its current derivative will double, leading to increased current ripple compared to the dual-inductor configuration.

**Sizing Considerations**

While transistor sizing is beyond the scope of this paper, two key factors affecting transistor ratings are worth considering: switching frequency and maximum current. As described earlier, the maximum current carried by the H-Bridge (HB) switches equals the source current $I_d$. Since the HB switches determine the polarity of the output current, they commutate at the fundamental frequency, toggling with each half-cycle of the output current. Switch pairs {S11,S14} and {S21,S24} direct inductor currents iL1 and iL2 to and from the load, respectively, and thus carry a maximum current equal to half the source current, $I_d/2$. These switches operate at the carrier frequency.

The characteristics described above are summarized in Table 2, where $f_0$ and $f_\Delta$ denote the fundamental and carrier frequencies, respectively.

**Table 2 Sizing factors**

| Switches | Maximum Current | Switching Frequency | Role |
|---|---|---|---|
| $S_{12}, S_{13}, S_{22}, S_{23}$ | $I_d$ | $f0$ | HB |
| $S_{11}, S_{14}, S_{21}, S_{24}$ | $I_d/2$ | $f\Delta$ | non-HB |

Since the power loss in a switch is directly proportional to the product of the current flowing through it and its switching frequency, the combination described above allows for a moderate rating selection for both HB and non-HB switches.

## 3. Simulation Verification

A Simulink/MATLAB R2023b model was developed to verify the operation of the proposed converter. Sine-PWM (SPWM) was employed to generate the gating signals for the transistors. For simplicity, the DC current source was modeled using an ideal 15 V DC voltage source in series with a 100 mH inductor. The simulation parameters are summarized in Table 3.

Table 3 Simulation parameter summary

| Parameter | Value | Units | Comments |
|---|---|---|---|
| $f0$ | 50 | Hz | Fundamental frequency |
| $f\Delta$ | 1050 | Hz | Carrier frequency |
| $V_S$ | 15 | $V_{DC}$ | Source voltage |
| $L_S$ | 100 | mH | Source inductance |
| $R_{load}$ | 22.5 | Ω | Load resistance |
| $C_f$ | 140 | uF | Filter capacitor |

For normal inverter operation, balancing the inductor currents iL1 and iL2iL2iL2 is essential. This was achieved using a simple hysteresis control that applied the balancing rule outlined in Section 2.2. Figure 3 displays the inverter output current $i_{INV}$ and the inductor currents iL1 and iL2. As anticipated, the inverter output current shows five discrete levels, while the inductor currents iL1 and iL2 fluctuate around their 1 A DC level.

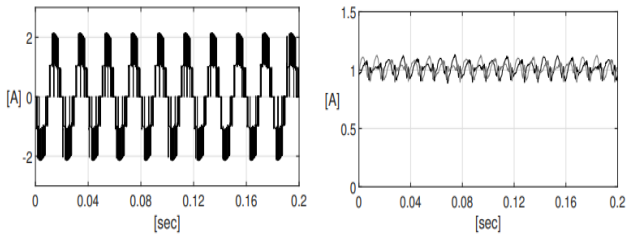



Figure 3 Simulated results for inverter current $i_{INV}$ and inductor currents iL1 and iL2.

Figure 4 illustrates the load voltage $v_o$ in both the time and frequency domains. As shown in Figure 4a, $v_o$ exhibits a sinusoidal waveform with a low dv/dt and a peak voltage of 30 V. Considering the 15 V DC source, the increased output voltage partially demonstrates the voltage boosting capability of the proposed inverter. A detailed analysis of the inverter's voltage boosting ratio and the modulation scheme used to achieve it is beyond the scope of this paper and will be covered in a future publication.

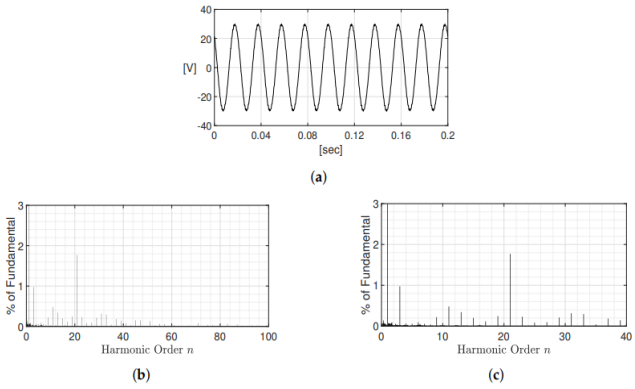


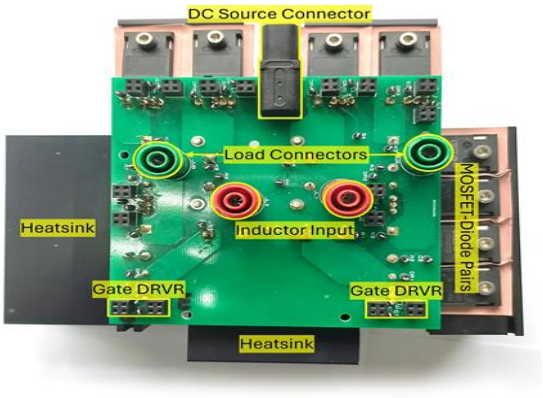

Figure 4 Simulated results for the load voltage vo in the (a) time domain, (b) frequency domain—100 lower harmonics, and (c) frequency domain—40 lower harmonics.

The normalized harmonic content of the load voltage is illustrated in Figures 4b and 4c. Analysis of these figures reveals two key features: First, there is a prominent 21st-order harmonic component with an amplitude of about 1.75% of the fundamental frequency, consistent with the 1050 Hz carrier frequency listed in Table 3. Second, a normalized third harmonic component with an amplitude of 1% is observed, resulting from low current oscillations due to the inverter's interaction with the current source (a DC voltage source in series with a choke inductor). The total harmonic distortion (THD) of the load voltage was measured at 2.28%.

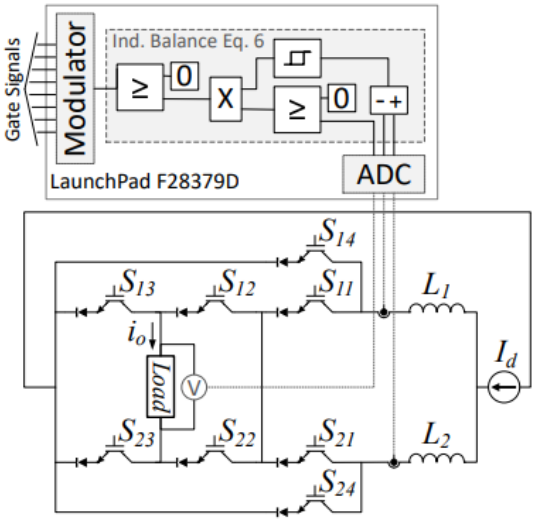
## 4. Experimental Verification

This section presents selected experimental results to validate the theoretical and simulation findings. All waveforms were captured using an R&S RTM3000 oscilloscope and imported into MATLAB for spectral analysis and figure generation. Current and voltage waveforms were measured using Keysight's current probe N2893A and voltage probe N2791A, respectively. The experimental setup is shown in Figure 5. The functional performance of the proposed inverter was tested with a SiC-MOSFET-based laboratory prototype, as depicted in Figure

5a. The inverter was implemented on a two-layer 100 mm × 100 mm PCB. To allow for testing flexibility, the load, inductors, and DC source were kept external to the switching circuit and connected via designated connectors. The two-layer PCB design facilitated perpendicular connections of the gate driver boards to the motherboard through connectors located near the MOSFET's source and drain terminals. As in the simulation, the current source was implemented using a laboratory DC voltage source of 15 V in series with a 100 mH choke inductor. The experimental parameters are summarized in Table 4.




(a)




(b)

Figure 5 Single-phase five-level CSI laboratory setup depicting (a) converter laboratory prototype and (b) schematic of the controller and sensor configuration

Inductor current balancing was achieved using the scheme described in Section 2.2. Load voltage and inductor current measurements were taken using LEM's current transducer LA55-P and voltage transducer LV25-P, respectively. These measurements were then input into the ADC module of a TI F28379D evaluation board, where a simple hysteresis control was implemented. For the voltage measurement, additional shift-and-scale circuitry was used to adjust the voltage transducer's AC output to the ADC's acceptable input range. The balancing index was subsequently fed into a PWM modulator to generate gate signals S11, S14, S21, and S24, as specified in equation (6).

Table 4 Experimental parameter summary

| Parameter | Value | Units | Comments |
|---|---|---|---|
| $f0$ | 50 | Hz | Fundamental frequency |
| $f_\Delta$ | 1050 | Hz | Carrier frequency |
| $t_{dt}$ | 0.5 | us | Off-delay |
| $V_S$ | 15 | $V_{DC}$ | Source voltage |
| $L_S$, $L_1$, $L_2$ | 100 | mH | Source and coil inductances |
| $R_{load}$ | 22.5 | Ω | Load resistance |
| $C_f$ | 140 | uF | Filter capacitor |
| *SiC MOSFET* | *C3M0065100K* | | Wolfspeed |
| *Curretn probe* | *N2893A* | | Keysight |
| *Voltage probe* | *N2791A* | | Keysight |
| *Controller* | *F28379D* | | C2000 Delfino MCU |
| *Diode* | *C4D10120D* | | Wolfspeed |
| *Current transducer* | *LA55-P* | | LEM |
| *Voltage transducer* | *LV25-P* | | LEM |

Figure 6 presents the experimental waveforms for the inverter output current $i_{INV}$ and the inductor currents iL1 and iL2. As observed in the simulation, $i_{INV}$ displays five discrete levels. Similarly, the inductor currents iL1 and iL2 fluctuate around a 1 A average, though their peak-to-peak values are notably larger than those in the simulation. This discrepancy arises from low-frequency oscillations in the source current, combined with measurement and quantization errors. These errors are attributed to sensor inaccuracies, shift-and-scale distortions, and electromagnetic interference (EMI) from the inverter. The observed current fluctuations reflect the inverter's operational characteristics and contribute to increased harmonic content in its output current. To address this, increasing the inductances and operating the inverter in closed-loop mode can help mitigate these effects.

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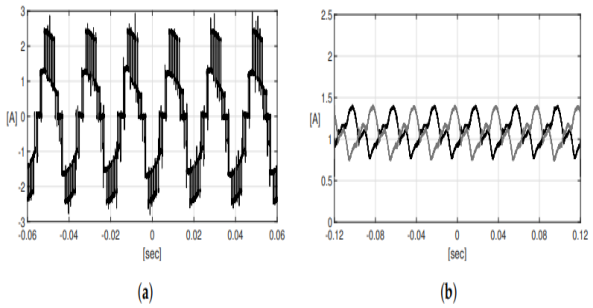


Figure 6 Experimental results for (a) inverter current iINV and (b) inductor currents iL1 (black) and iL2 (grey)

Figure 7 illustrates the load voltage $v_o$ in both the time and frequency domains. As shown in Figure 7a and consistent with the simulation results presented in Section 3, $v_o$ exhibits a sinusoidal waveform with a low dv/dt and a peak voltage of 30 V. The 15 V DC input is effectively amplified to a 60 V peak-to-peak output voltage, highlighting the inverter's voltage boosting capability.

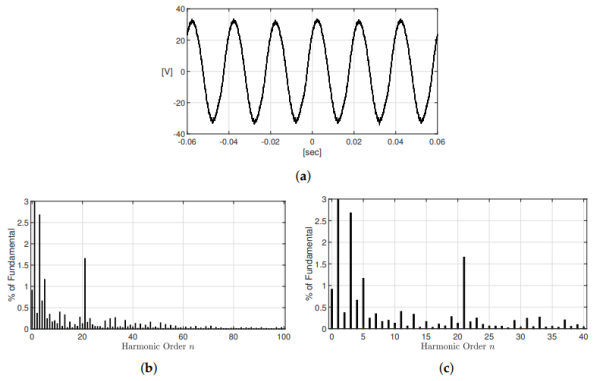


Figure 7 Experimental results for load voltage vo in the (a) time domain, (b) frequency domain—100 lower harmonics, and (c) frequency domain—40 lower harmonics

The normalized harmonic content of $v_o$ is presented in Figures 7b and 7c, which display 100 and 40 lower-order harmonics of the output voltage, respectively. Consistent with the simulation results, the dominant harmonic component of the output voltage occurs at the switching frequency, amounting to 1.65% of the fundamental amplitude. The load voltage exhibits a total harmonic distortion (THD) of 3.7%, which is higher than that observed in the simulation. This increase is due to larger fluctuations in the inductor currents caused by less precise inductor balancing and measurement and quantification errors in the control system. These fluctuations also disrupt the symmetry of the inverter current, resulting in a minor DC component, as shown in Figures 7b and 7c.

As indicated in Table 1, the following relations apply in the case of zero off-delay.

$$S_{11} = \overline{S_{14}},\ S_{12} = S_{23},\ S_{21} = \overline{S_{24}},\ S_{22} = S_{13} \tag{11}$$

From equation (11), and disregarding the off-delay effect, switches S11, S12, S21, and S22 provide a comprehensive view of the inverter's switching states and directly determine the states of the other four switches. Therefore, only four gate waveforms need to be acquired. Figure 8 presents the gating signals for switches S11, S12, S21, and S22. As described, and ignoring the off-delay effect, these waveforms match those of switches S14, S23, S24, and S13, respectively. For measurement convenience, all waveforms were captured at the ePWM pins of the TI F28379D controller board. Figures 8a and 8c show the gating signals for switches S11 and S21. According to the analysis in Section 2.3, these switches, along with their complementary switches S14 and S24, operate at the carrier frequency. Figures 8b and 8d illustrate the gating signals for switches S12 and S22. These switches, and their counterparts S23 and S13, operate at the low fundamental frequency. Switches S11 and S21 (and thus S14 and S24) handle half the source current and switch at the high carrier frequency. Conversely, switches S12 and S22 (and S13 and S23) carry the full source current and switch at the low fundamental frequency. This confirms the analysis presented in Table 2. Since switching loss is proportional to the product of the current and the switching frequency, these observations suggest a relatively moderate rating for both HB and non-HB switches.

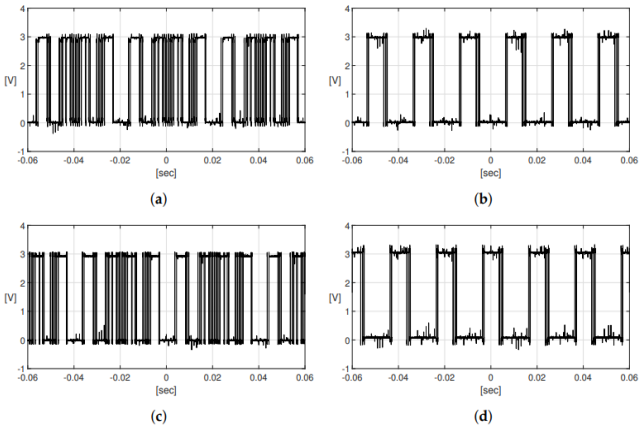


Figure 8 Controller board gating signals for switches (a) $S_{11}$, (b) $S_{12}$, (c) $S_{21}$, and (d) $S_{22}$

It is important to note the additional commutations of switches S12 and S22 near the zero crossing of the inverter output current. These extra commutations arise from switching between zero and intermediate current states of ±Id/2. This issue can be completely eliminated by implementing a conditional switching rule that aligns the appropriate HB switching state with each half-current cycle.

## 5. Conclusion

In this study, we introduced and thoroughly analyzed a novel single-phase five-level Current Source Inverter (CSI) topology that incorporates eight switches and two DC link inductors. This innovative design successfully generates five distinct current levels at the inverter's output while ensuring a symmetrical structure with even current distribution between the inductors. The proposed CSI also demonstrates the flexibility to operate in a single-inductor mode, though this configuration results in a doubling of the inductor current ripple. The comprehensive analysis covered the inverter's functional operation, including its switching states and conduction paths. We detailed the dynamics of inductor currents and provided a robust algorithm for balancing them, verified through both theoretical analysis and practical implementation. The use of redundant switching states effectively maintains inductor current balance, and a specific mechanism for balancing inductor currents in single-inductor mode was presented. The inverter's design features an H-Bridge (HB) submodule that facilitates polarity reversal of the output current. The operational analysis showed that the HB switches commutate at the low fundamental frequency while handling the full source current, whereas the non-HB switches operate at the higher carrier frequency with half the source current. This distribution minimizes switching losses and supports moderate switch ratings. Simulation and experimental results, including open-loop operation and hysteresis control for inductor current balancing, confirmed the theoretical predictions. The prototype demonstrated a voltage boost ratio of 1:4, showcasing the inverter's voltage boosting capability. Future research will focus on advancing to closed-loop operation, refining loss modeling, and exploring enhanced modulation techniques to further optimize the inverter's performance.

## References

[1] Harkiran, S.J., Saxena, S.A., Sharma, S., and Singh, A. Zero Emission Vehicles (ZEVs): Towards a Policy Framework. NITI Aayog & World Energy Council, 2018.

[2] Zhang, F., Zhang, X., Zhang, M., and Edmonds, A.S.E. "Literature Review of Electric Vehicle Technology and Its Applications." 5th International Conference on Computer Science and Network Technology (ICCSNT), 2016, pp. 832-837.

[3] Biswas, S., Behera, S., Choudhury, N.B.D., Goyal, S.K., Palwalia, D.K., Tiwari, R., and Gupta, Y. "A Brief Review on the Barriers of Electric Vehicle Adoption and Present Scenario in India." Flexible Electronics for Electric Vehicles (FLEXEV 2022), vol. 1065, Springer, Singapore, 2024,

[4] Totev, V., and Gueorgiev, V. "Efficiency of Regenerative Braking in Electric Vehicles." 21st International Symposium on Electrical Apparatus & Technologies (SIELA), 2020, pp. 1-4.

[5] Hamid, J., Sheeba, R., and Sofiya, S. "Energy Harvesting Through Regenerative Braking Using Hybrid Storage System in Electric Vehicles." IEEE International Conference on Intelligent Techniques in Control, Optimization and Signal Processing (INCOS), 2019, pp. 1-6.

[6] Owusu, P.A., Asumadu-Sarkodie, S., and Dubey, S. "A Review of Renewable Energy Sources, Sustainability Issues and Climate Change Mitigation." Cogent Engineering, vol. 3, no. 1, 2016,

[7] Viswanathan, V., and Jeevananthan, S. "Hybrid Converter Topology for Reducing Torque Ripple of BLDC Motor." IET Power Electronics, vol. 10, 2017, pp. 1572-1587.

[8] Barros, L.A.M., Martins, A.P., and Pinto, J.G. "A Comprehensive Review on Modular Multilevel Converters, Submodule Topologies, and Modulation Techniques." Energies, vol. 15, no. 3, 2022, p. 1078.

[9] Choudhury, S., Bajaj, M., Dash, T., Kamel, S., and Jurado, F. "Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects." Energies, vol. 14, no. 18, 2021, p. 5773.

[10] Singh, K., and Pathak, M.K. "An Improved Two-Stage Non-Isolated Converter for On-Board Plug-In Hybrid EV Battery Charger." IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 2016, pp. 1-6. IEEE,

[11] ana, R.A., Patel, S.A., Muthusamy, A., Cw, L., and Kim, H.-J. "Review of Multilevel Voltage Source Inverter Topologies and Analysis of Harmonics Distortions in FC-MLI." Electronics, vol. 8, no. 11, 2019, p. 1329. MDPI.