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# Multi-Level Inverter with Reduced Device Count for Energy Systems

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***Abstract:*** *In this study, a new multilevel converter topology is suggested. The suggested topology's key characteristics are its low component count and compact design. The suggested converter also lacks capacitors, inductors, and diodes, which allows for a smaller converter footprint, longer converter lifetime, and easier control method. In addition, a comparison with current multilevel topologies is done to illustrate the advantages of the proposed circuit. A presentation of the simulation results for the three-level version utilising various modulation schemes follows.*

**Keywords:** *pulse width modulation multilevel inverters, fundamental frequency modulation, THD.*

## 1. Introduction

In order to meet the rising demand for energy around the world while limiting CO2 emissions, renewable energy generators (REGs) are becoming more heavily incorporated into the grid. As a result, considerable reductions in CO2 emissions and notable advancements in energy saving are made. To improve system dependability and effectiveness, however, new technological proposals are constantly needed. The requirement for better power electronics converters (PECs), which connect the primary energy source to the grid, has increased as a result of recent advancements in those technologies. In power systems with renewable generators, PECs are crucial because they transform the generated primary power from REGs to be in compliance with the grid or load regulations. PECs are also used to improve the efficiency of generating systems due to their capacity to integrate various storage technologies, which enables them to perform a number of crucial tasks like energy arbitrage, peak shaving, load-flowing, spinning reserves, voltage support, black starts, frequency regulation, etc. [1].

Photovoltaic (PV), wind, and hydropower plants (HPP) are the main types of REGs. Different converter families, including conventional voltage source converters (VSCs), matrix converters (MCs), and cyclo-converters (CCVs), have been utilised in these generating systems for a very long period. However, significant issues with these converters include limited power handling caused by the maximum power ratings of semiconductor devices that are currently available, high total harmonic distortion (THD) on the input and output sides, and a negative impact on the system's power factor when using converters that are not fully controlled, like CCV [2-5]. For the purpose of overcoming the aforementioned restrictions, a number of solutions have been put forth, including the use of identical converters in parallel configurations to increase the handled power, the use of elaborate, large, and specially designed filters to improve THD, and the use of compensation circuits to control reactive power and enhance power factor in converters that are not fully controlled. However, these approaches are currently losing their appeal because they make PECs heavier, more complex, and more expensive, while also reducing the effectiveness, dependability, and lifespan of the energy system [2, 3, 5]. These limitations stop these converters from being used in high power applications. Multilevel converters (MLCs) are employed extensively in contemporary medium- and high-power energy systems because to their special characteristics of modularity, low dv/dt, low THD, low switching frequency, low electromagnetic interferences, minimal filtering requirements, and low switching losses [6–8]. Or to put it another way, systems based on MLCs generate high-quality outputs with manageable side effects.

Three typical topologies of MLCs are the cascaded H-bridge converter (CHB) [13], the flying capacitors converter (FC) [11, 12], and the neutral point clamped converter (NPC) [9, 10]. The fundamental disadvantage of

the aforementioned topologies is their high component count, which includes DC sources, electrolytic capacitors, transformers, switching devices, and power diodes. This increases the footprint, cost, conduction losses, control complexity, and lifetime of the converter [6–8]. A number of topologies were recently given in [14–20] with the intention of improving traditional setups by recommending new circuits with fewer components and easier control methods. This research proposes a new multilevel converter topology with this objective in mind. In comparison to the current setups, the proposed architecture can generate the same number of voltage levels with a less component count. The proposed topology also offers a compact design feature since it doesn't operate by using electrolytic capacitors or transformers. This portable solution's small size and minimal cooling system requirements are made possible by this feature's compactness. Additionally, the suggested circuit's losses will be drastically reduced because it uses solely switching devices that operate at low frequencies rather than hybrid designs that combine switches and diodes.

The structure of this essay is as follows. In part II, the proposed topology's operational principles for a three-level setup will be provided. The suggested circuit will be compared to various MLC topologies for producing the same number of voltage levels in section III. Then, part IV will discuss the two switching techniques that have been used, and section V will present the outcomes of the simulations for the two modulation techniques. In section VI, conclusions will be retracted.

## 2. Proposed Multi-Level Converter Topology

Designing the proposed MLC topology had as its primary goal the simplification of the converter construction. This allows for the adoption of a straightforward control system and increases reliability to a greater extent. In order to avoid enlarging the converter's size, incurring losses, or shortening its lifetime, the design of the suggested topology shouldn't include electrolytic capacitors, power transformers, or power diodes. Additionally, the input DC ports need to be shrunk for larger applications. Therefore, fewer isolated DC sources will be needed, which will save costs. Typically, a six-pulse rectifier and an isolation transformer define one DC source. Saving one DC source translates into saving six power diodes and one isolation transformer, respectively. This viewpoint claims that the suggested topology is built to have fewer isolated DC sources while maintaining a manageable switching device count. The suggested design generates three-level pole voltages from just two DC sources and twelve switching devices, culminating in five-level line voltages. For instance, two PV generators can be used to create the two isolated DC sources. The suggested MLC's power circuit and consequent voltages are shown in Fig. 1. Even though the proposed topology can be expanded to N levels, this work only studies the three-level setup.

Pole voltage will be used to refer to the voltage differential between point A, B, or C and point 0 throughout this essay. Both line and phase voltages can be synthesised using the pole voltages $V_{A0}$, $V_{B0}$, and $V_{C0}$. In order to produce three-level voltage waveforms with 120° phase shifts, both switching techniques are built to control the switches that are used. As a result, it is possible to create five-level line voltages, as demonstrated in Fig. 1(b), where the line voltage VAB is created by deducting $V_{A0}$ from $V_{B0}$.

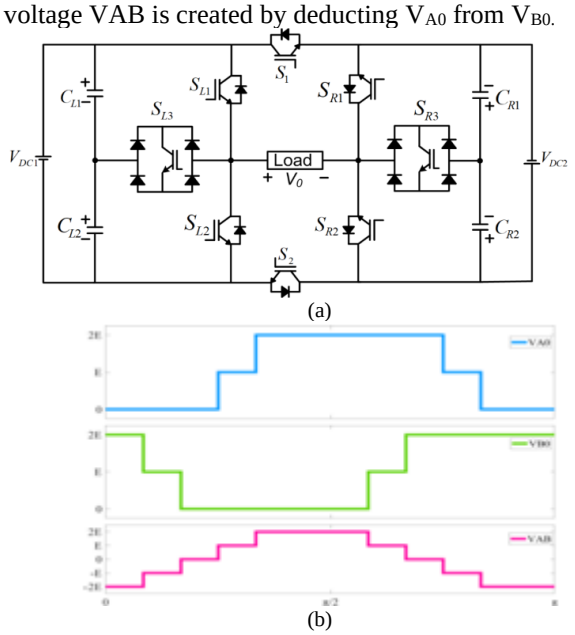



Fig. 1. The proposed three-phase multilevel topology. (a) The power circuit for the proposed topology. (b) Line voltage $V_{AB}$ synthesization using pole voltages $V_{A0}$ and $V_{B0}$.

## 3. Comparison of the Proposed Topology With Other MLC Topologies

As indicated in section I, conventional multi-level converters like the CHB, FC, and NPC suffer from a number of control and component count issues. New and modified topologies have been documented in [14–20] to get around these restrictions. These topologies seek to reduce the number of components while boosting

effectiveness and dependability. Despite the fact that these configurations are frequently utilised in industrial applications, some of them are still undergoing research and development. The findings of a comparison technique about the components necessary to generate an equivalent number of voltage levels are summarised in Table I. The following unified restrictions form the foundation of the comparative strategy: generating three-level pole voltages for each topology while only employing symmetrical DC sources, i.e. counting a DC voltage source with a rating of 2E as two separate DC sources, and converting single-phase topologies into three-phase versions before comparison.In terms of the component count at the same voltage levels and the given limitations, Table I compares the proposed topology to known circuits in the literature. Comparing the suggested architecture to the existing three-level topologies, it may provide the same output voltage levels while utilising less components. The absence of capacitors, diodes, and inductors is the suggested topology's key benefit, as it enables the proposed MLC to have a longer lifespan, lower switching losses, and a compact design. The next paragraphs emphasis and describe the primary traits and constraints of the comparative topologies.

A three-level topology was introduced in [20], which is an expansion of the split-source inverter (SSI) with two levels that was described in [21]. It has a boosting feature that enables it to provide a high-quality three-level output voltage, facilitating the direct connection of low-voltage energy sources like photovoltaics (PV). One DC supply, twelve semiconductor switches, three power diodes, four capacitors, and just one inductor are needed to generate three levels. Although this topology has features like multi-level outputs, boosting capability, and operating with a single source, it has drawbacks like high current and voltage stresses on the used semiconductor components, a limited capacity for power transfer, an increased system footprint due to capacitors and inductors, increased control complexity due to these components, and a shorter expected lifetime of the converter.

Additionally, the output voltage's quality depends on the gain value; for example, for low input voltages, increasing the output voltage causes a rise in THD. Additionally, it requires additional work in the control algorithms to eliminate the low-frequency components brought on by oscillations in the voltages of flying capacitors, both in the input current and the output voltage. Additionally, in grid-connected mode, using soft-start-up resistors is required to limit switch voltage stress during startup, while in stand-alone mode, controlling these issues can be done in part by setting control parameters in the control algorithm.

Table I. Comparison Between the Proposed Topology and Three-Level MLC Topologies

| Topology | DC Sources | Switches | Diodes | Capacitors | Inductors | Total | CLF [a] |
|---|---|---|---|---|---|---|---|
| Modified T-type [19] | 1 | 9 | 12 | 2 | 0 | 24 | 8.0 |
| Fig. 8 in [16] | 3 | 9 | 9 | 0 | 3 | 24 | 8.0 |
| In [18] | 1 | 18 | 0 | 3 | 0 | 22 | 7.3 |
| Neutral point clamped (NPC) | 1 | 12 | 6 | 2 | 0 | 21 | 7.0 |
| Active T-type converter [14, 17] | 1 | 18 | 0 | 2 | 0 | 21 | 7.0 |
| In [20] | 1 | 12 | 3 | 4 | 1 | 21 | 7.0 |
| Cascaded half H-Bridge (CHHB) | 6 | 12 | 0 | 0 | 0 | 18 | 6.0 |
| Flying capacitors (FCs) | 1 | 12 | 0 | 4 | 0 | 17 | 5.7 |
| Cascaded full H-bridge (CHB) | 3 | 12 | 0 | 0 | 0 | 15 | 5.0 |
| T-type converter [14, 19] | 1 | 12 | 0 | 2 | 0 | 15 | 5.0 |
| Fig. 5 in [15] | 3 | 9 | 3 | 0 | 0 | 15 | 5.0 |
| The proposed topology | 2 | 12 | 0 | 0 | 0 | 14 | 4.7 |

Authors in [18] have highlighted a new MLC that uses multiple sets of anti-parallel switches for the level-generator stages in addition to two primary switches to adjust the polarity of the output voltages. This configuration needs 18 switches, 3 capacitors, and 1 DC source to generate three-level three-phase voltage. The main drawbacks of this circuit include the use of electrolytic capacitors to divide a single DC source into three equal parts, the necessity of a large number of switches, and high voltage stress across switches used to change polarity, which causes a variety of losses and heat distribution inside the converter. As a result, the system lifetime is shortened while the converter cost, size, losses, and control complexity rise.

In [15], a dual-DC-port asymmetrical MLI (DPAMLI) was created and studied. To produce three-level voltage for three-phase applications, nine switches, three power diodes, and three DC sources (two with E and one with 2E) are needed. For the purpose of deriving the proposed topology, the neutral point clamped (NPC) and T-type three-level cells are utilised. Despite the fact that the DPMLI can support bidirectional power flow between input and output ports, only a unidirectional version was highlighted and confirmed in [15] with the intention of lowering the number of components. It is a single-stage converter that can be used to connect two DC sources of various ratings and can generate AC output voltages with several levels. This facilitates and improves the efficiency of connecting several voltage sources to a single converter. It has two operating modes, and the controller chooses one of them depending on how much voltage is actually

delivered across the low DC port terminals in proportion to the needed output voltage. Although it has no issues using electrolytic capacitors, it also employs power diodes, which increases converter losses. This topology can only be used in low- and medium-voltage systems since at least six switches have high voltage stresses equal to the voltage delivered across the high-voltage DC port terminals.

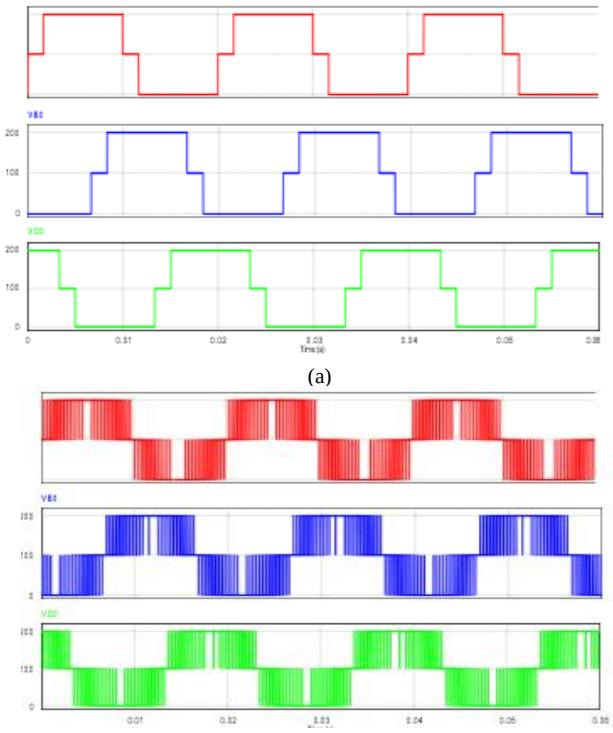
The authors of [19] have developed a modified three-level topology of the well-known T-type MLI with the aim of reducing switch count. A cell made up of one switch and four diodes was used in place of the three bidirectional switches that connected the load points and the clamped neutral point. Two capacitors, one DC source, twelve power diodes, nine switches, and a typical T-type architecture are required for this topology to produce the same output voltage levels. For many applications that need great efficiency, durability, and small size, this topology is unappealing due to the use of capacitors and a significant number of semiconductor components.

## 4. Simulation Results and Discussions

A three-level model is created and simulated for both a pulse width modulation technique and a fundamental frequency modulation in order to demonstrate the operation of the suggested architecture. To provide a three-level pole voltage, the simulated model employs twelve switches (nine of E volt and three of 2E volt) and two symmetrical DC voltage sources. The primary simulation settings are provided in Table II, and the simulation results were obtained using the PSIM software.
When the suggested converters are modulated by SCM and LSPWM switching techniques, the pole voltages VA0, VB0, and VC0 are shown in Fig. 2. Five-level balanced three-phase line voltages VAB, VBC, and VCA will be produced at the load terminals by maintaining the voltage across pole terminals have three steps and a phase shift of 120°, as illustrated in Fig. 3. The simulation results for the suggested topology when powering a resistive-inductive load with a power factor of 0.9 are shown in Fig. 4.

Table 2. Simulation System Main Specifications

| System parameters | Value |
|---|---|
| DC voltage value E | 100 V |
| Load value at 50 Hz | $R$= 50 Ω, $X_L$= 23.6 Ω |
| Switching Frequency $F_s$ | 2.5 kHz |
| Modulation index Mi (= $Sin_M$ / $C_{RM}$) | 1 |

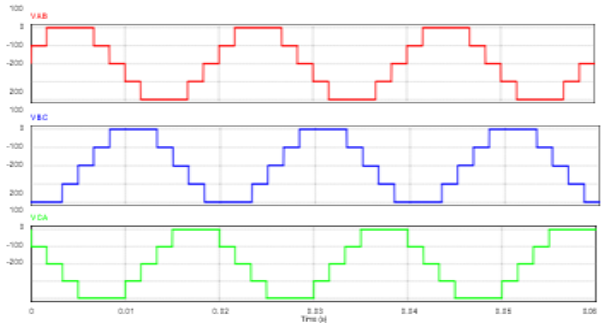


(a)

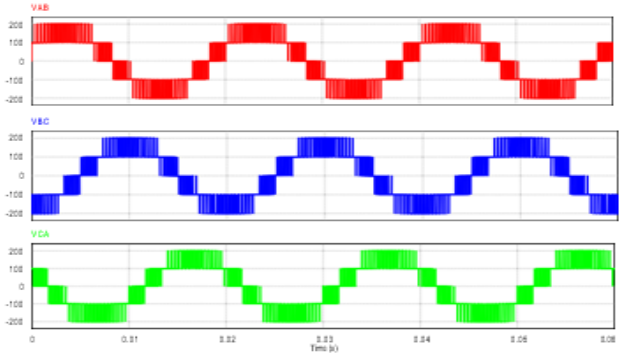
(b)

Fig. 2. The pole voltage waveforms: $V_{A0}$, $V_{B0}$, and $V_{C0}$. (a) staircases modulation. (b)Level-shifted PWM

It can be seen that the voltage level number differs between the two graphs for VAN in Fig. 4(a) and (b), which is compatible with the used switching strategy. There are nine levels of -4/3 E, - E, -2/3 E, -1/3 E, 0, 1/3 E, 2/3 E, E, 4/3 E for LSPWM and seven levels of -4/3 E, - E, -2/3 E, 0, 2/3 E, E, 4/3 E for SCM in VAN. When adopting the LSPWM switching scheme, two new voltage combinations in the pole voltages result in the generation of the two additional voltage levels in VAN 1/3 E. More information on the impact of switching strategies on the phase voltage level number is given in Tables III.

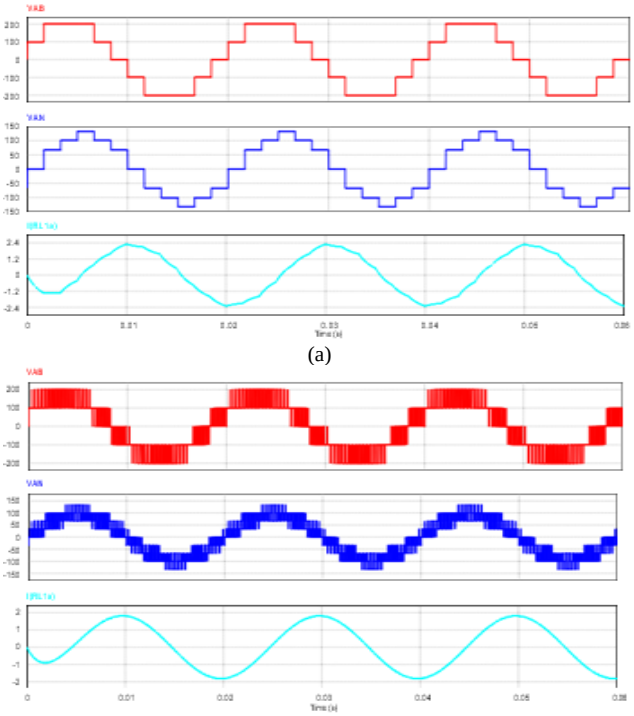


(a)



(b)

Fig. 3. The output line voltage waveforms: $V_{AB}$, $V_{BC}$, and $V_{CA}$. (a) Staircases modulation. (b) Level-shifted PWM.



(a)

(b)

Fig. 4. The output waveforms under R-L load: $V_{AB}$, $V_{An}$, and $I_{An}$. (a) Staircasesmodulation. (b) Level-shifted PWM.

Table 3. The Switching Modulation Effects on the Number of Levels of the Phase Voltage Van

| $V_{A0}$ | | $V_{B0}$ | | $V_{C0}$ | | $V_{AN}$ | |
|---|---|---|---|---|---|---|---|
| SCM | LSPWM | SCM | LSPWM | SCM | LSPWM | SCM | LSPWM |
| 2E | 2E | 0 | 0 | 0 | 0 | 4/3 E | 4/3 E |
| 2E | 2E | E | E | 0 | 0 | E | E |
| 2E | 2E | 2E | E | 0 | E | 2/3 E | 2/3 E |
| - | E | - | E | - | 0 | - | 1/3 E |
| E | E | 2E | 2E | 0 | 0 | 0 | 0 |
| - | E | - | 2E | - | E | - | -1/3 E |
| 0 | 0 | 2E | 2E | 0 | 0 | -2/3 E | -2/3 E |
| 0 | 0 | 2E | 2E | E | E | -E | -E |
| 0 | 0 | 2E | 2E | 2E | 2E | -4/3 E | -4/3 E |

## 5. Conclusion

In this work, a brand-new three-level multilevel inverter is suggested and examined. Without the use of any passive components, the suggested topology is capable of producing a three-level pole voltage. In comparison to other three-level topologies that are already in use, it also requires less components. For the purpose of creating three balanced three-phase output voltages, two modulation techniques based on fundamental frequency modulation and sinusoidal pulse width modulation are successfully used. A simulation model of the circuit and the resistive-inductive load is used to confirm the effectiveness of the suggested topology. Additionally, a comparison study is conducted to demonstrate the benefits of the suggested circuit, offer insight into the trade-offs in design, and determine the best multilevel converter topologies.

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