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A Literature Review on Rail to Rail Buffer Amplifier

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Abstract: *An operational amplifier is one of the most basic components in analog, mixed signal, RF, and other integrated circuit designs. Analog Devices high speed (> 50 MHz) rail-to-rail op amps enable you to operate at lower supply voltages, swing closer to the rails, and provide wider dynamic range. Featuring a portfolio with a wide variety of op amps, including both rail-to-rail input/output as well as just rail-to-rail output, ADI provides the widest portfolio of leading edge products available on the market. Whether it is wide bandwidth, high slew rate or low distortion, or rail to rail, no one sets more performance standards for next generation designs than Analog Devices. In this paper, we present the review of literature work done by the various researchers in this area.*

Keywords: *Rail-to-Rail buffer, Op-Amp amplifier, CMOS technology, FCTA, Transconductance.*

1. Introduction

An operational amplifier is one of the most commonly used components in analog and digital circuit designs. It is found in applications such as communications transmitters and receivers, medical devices, and multimedia electronics. In each of these applications, the need for low voltage low power amplifiers has steadily increased as many devices shift toward portable and battery powered operations. It is the main goal in low power amplifier designs to maintain an acceptable level of performance as supply voltages continue to drop for these applications. [1] In general, for CMOS VLSI technology, as the supply voltage and current decrease, the performance of the transistor degrades. This degradation necessitates research and exploration for low voltage and low power design techniques to compensate for the loss in performance due to reductions in supply voltages and currents. As the supply voltage and current of an analog circuit decrease there are certain performance measures of the circuit which will suffer a loss in performance. For example, for lower supply voltages the signal to noise ratio of the circuit will decrease, as the maximum input and output signal for the circuit will be smaller. Also the achievable bandwidth will be reduced as the supply voltage and total current are reduced. Less headroom tends to be available when the supply voltages are reduced. A reduction in headroom removes the possibility of using cascoded or stacked devices to increase the output impedance. In terms of the minimum usable supply voltage, it is required that the following expression is satisfied,

VDD > Vsignal_swing + K*VDsat,

Where VDsat is the minimum transistor saturation voltage, Vsignal_swing is the signal swing of the circuit, and K represents the number of transistors stacked in series. Thus, as the supply voltage decreases, the largest possible value of K will also decrease, which implies cascoding may become difficult or impractical. Each of the previous noted issues described will apply to all low voltage designs and should be considered at the design level; however there are more exclusive specifications which apply particularly to amplifier designs that will suffer as a result of reduced supply voltages. This includes such characteristics as DC gain, gain-bandwidth product, phase margin, and power consumption. In order to create a design in which these performance parameters do not degrade at low voltage, the cause of performance degradation must first be studied

2. Amplifier Characterization

There is several performance measures used to characterize all amplifiers. Some of the most commonly observed characteristics include the DC gain (AVO), gain-bandwidth product (GBW), phase-margin (PM), and power consumption. Other performance specifications used to characterize amplifiers include slew-rate, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), total harmonic distortion (THD), and the input noise voltage. At low voltages each of these performance measures becomes more sensitive to the design of the amplifier and characteristics of the process. [1] The theoretical limit of the minimum voltage that can be used to operate an amplifier is limited by the threshold voltages, which are characteristic of the process. Smaller feature size processes can be used (which have a lower threshold voltage) to achieve lower voltage operations. However, with smaller feature size processes, it becomes more difficult to optimize the performance measures mentioned above. In order to understand how an amplifier's performance measures are affected by low voltage implementation, it is important to first define each performance measure and explore which transistor parameters have the greatest affect on them.

The DC gain of an amplifier is one of the most commonly used performance measures. It is typically preferable for an operational amplifier to have a large DC gain, which will allow for better closed loop performance. The DC gain is the open loop gain from input to output of an amplifier at low frequencies. The DC gain of an amplifier mostly depends on the transconductance gain (gm) of the input pair and the output conductance (go) of the amplifier.[2-5] The transconductance gain expression is given by (1.1), where m is the mobility of the material, Cox is the gate oxide capacitance, W and L are the width and length of the transistor respectively, and IDQ is the transistor quiescent current. Similarly, the output conductance of a single transistor is given by (1.2), where l is the channel length modulation factor, VGS is the gate source voltage, and VT is the threshold voltage. It is seen from (1.1) and (1.2) that the DC gain of an amplifier will have several process dependent terms, namely m, l, and Cox. This implies that there are physical limitations due to the process when designing for a particular DC gain. Also it is observed that as these process variables vary randomly, the DC gain will be affected as a result. The gain-bandwidth product is also an important performance measure for all operational amplifiers. The GBW typically gives an indication of the relative speed of the amplifier. The GBW is given by the product of the DC gain and the bandwidth of the amplifier as the name suggest. The GBW often is compared to the unity gain frequency as these two values are usually in the same range. It is also desired to have an amplifier with a high GBW, which allows the amplifier to operate at higher speeds.[6] The GBW is highly dependent on the capacitive load (CL) that is present at the output as well as the transconductance gain of input stage. For multi-stage designs the GBW may also be limited by the compensation capacitor, however the transconductance gain remains a factor for this performance measure. As previously stated, gm has several process dependent terms and hence the GBW can also be affected by variations in process terms.

The phase-margin is a parameter that is used to determine the stability of an amplifier in closed-loop applications. It is typically desired to have a phase margin greater than 45° at the open loop unity gain frequency, which implies that there is 45 degrees of phase above a -180° phase delay. The phase margin of an amplifier is mostly dependent on the separation of the dominate poles of the system. For a multistage design this is controlled by the use of a compensation capacitor.[7-12] However the gain and the bandwidth of an amplifier will affect the phase margin significantly. For higher gains a large pole separation is necessary to achieve an acceptable phase margin. Also, the bandwidth gives an indication of what frequency the dominate pole lies and gives a hint about where the second dominate pole should be placed for the amplifier to be considered stable. Thus it is seen that as the gain and bandwidth of an amplifier change, the requirements for compensation to guarantee stability are also altered.

The power consumption of an amplifier is simply the amount of power the amplifier dissipates. The power consumption directly limits the maximum achievable GBW of the amplifier. Thus the GBW that will be observed is relative to the power which is consumed in the amplifier. When designing an amplifier, typically the power consumption is fixed and it is the goal of the design to maximize GBW based on this specification.

For the amplifier specifications mentioned it is important to understand how these specifications should be designed at low voltages. As stated previously, at low voltages the signal to noise ratio of an amplifier is reduced as the maximum input signal is smaller. This induces the need for rail-to-rail operations at low voltages. This implies that each of the amplifier's performance measures are kept relatively constant for common-mode values ranging from the negative supply (Vss) to the positive supply (Vdd). This allows for the input signal to be as large as possible, thus maximizing the signal to noise ratio. For low voltage amplifiers it is also necessary to obtain rail-to-rail differential outputs to maximize the signal to noise ratio.

In order to achieve a rail-to-rail operation, it is necessary to hold each of the amplifier's performances measures constant across the entire common-mode range. If the amplifier specifications are not held constant, the amplifier will exhibit an undesirable variation in performance as the common-mode changes. For example if the DC gain of an amplifier is different across the common-mode range, the phase margin of the amplifier will also vary. This can cause the amplifier to either become undercompensated/unstable or become overcompensated at a particular common-mode level. The same argument follows for the GBW. As previously mentioned, the DC gain as well as the GBW highly depends on the input gm and the output go of the amplifier. This implies that for low voltage amplifier designs, it is of interest to keep gm and go constant for the entire common-mode range in order to obtain a constant DC gain and GBW. There has been much work in creating design techniques to keep gm as constant as possible [13-15]. Less work has been explored to keep go constant, however it is an important topic when trying to design a rail-to-rail input/output amplifier in terms of maintaining a more constant DC gain. Exploring methods for keeping go constant also gives way to implementing commonly used gain boosting techniques for low voltage designs.

3. Literature Survey

Emre Arslan et al. (2015) a very compact, rail-to-rail, high-speed buffer amplifier for liquid crystal display (LCD) applications is proposed. Compared to other buffer amplifiers, the proposed circuit has a very simple architecture, occupies a small number of transistors and also has a large driving capacity with very low quiescent current. It is composed of two complementary differential input stages to provide rail-to-rail driving capacity. The push–pull transistors are directly connected to the differential input stage, and the output is taken from an inverter. The proposed buffer circuit is laid out using Mentor Graphics IC Station layout editor using AMS 0.35 µm process parameters. It is shown by post-layout simulations that the proposed buffer can drive a 1 nF capacitive load within a small settling time under a full voltage swing, while drawing only 1.6 µA quiescent current from a 3.3 V power supply.[16]

Chih-Wen Lu and Ching-Min Hsiao (2011) A high-speed low-power rail-to-rail buffer amplifier, which is suitable for liquid crystal display driver applications, is proposed. An offset voltage is intentionally built in the second stage to cut off the transistors of last stage from the output node in the stable state and hence achieve low dc power consumption. The input referred offset voltage due to the built-in offset is very small. The buffer draws little current while static but has a large driving capability while transient. An experimental prototype buffer amplifier implemented in a 0.35µm CMOS technology demonstrates that the circuit can operate under a wide power supply range. Quiescent current of 5 µA is measured. The buffer exhibits the settling time of 1.5µs for a voltage swing of 0.1~(VDD~0.1)V under a 600 pF capacitance load. The area of this buffer is 30x98µm^2. The measured data show that the proposed output buffer amplifier is very suitable for LCD driver applications [17].

Rien Beal (2009) An operational amplifier is one of the most basic components in analog, mixed signal, RF, and other integrated circuit designs. Low voltage and low power operational amplifier design has become an increasingly interesting subject as many applications switch to portable battery powered operations. The need for design techniques to allow amplifiers to maintain an acceptable level of performance when the supply voltages are decreased is immense. One of the most important features in low voltage amplifier designs is ensuring that the amplifier maintains constant behavior in the presence of rail-to-rail input common mode variations while providing a rail-to-rail output to maximize signal-to-noise ratio. In this work a new rail-to-rail low voltage operational amplifier is designed, simulated, and compared against state of the art amplifier designs. The amplifier architecture aims at achieving constant amplifier operation over a rail-to-rail common-mode input voltage range. The concept of constant operation refers to the ability to maintain constant specifications such as gain, gain-bandwidth product, phase margin, slew rate, and power consumption against large variations in input common-mode voltage. The amplifier is additionally designed to be robust with respect to variations in process parameters, supply voltages, and operating temperatures (PVT). A final evaluation of the performance of the proposed design versus that of the state of the art in the open literature is carried out. The intended capabilities and advantages of the new design are verified through extensive simulation [18].

Mezyad M. Amourah, Saqib Q. Malik, Randall L. Geiger (2005) A design technique for rail-to-rail operational amplifiers is presented. The technique adds dummy pairs to sense the common mode range of the input differential pair and adjusts the output current accordingly. An amplifier built in the TSMC 0.25µ process shows a DC gain of approximately 84dB. The amplifier provides high

gain for a wider range of output voltages. Design considerations for reducing the impact of the additional circuitry on the core are provided. The technique described can be adapted for use with traditional fully-differential rail-to-rail amplifiers [19].

Sadhana Sharma and Shyam Akashe (2013) A rail-to-rail high speed buffer amplifier is proposed with power gating technique, which is used for flat panel displays. By using power gating technique buffer amplifier has achieved the reduced leakage power by more than two orders of magnitude. The presented buffer amplifier is the combination of two transconductance amplifiers, two current comparators, A push-pull output stage and two sleep transistors. The buffer amplifier is simulated at the 45nm technology with cadence software at 3v supply voltage. The leakage current of this circuit is reduced by 4% (i.e. .79×10-6μA). The settling time for a rail-to-rail buffer swing is settled down to the range of .299×10-6μA.

Soo-yang Park et al. (2009) A structural rail-to-rail high voltage CMOS buffer amplifier for driving gamma correction reference voltage of TFT LCD panels is presented. It operates from a single supply and only consumes 0.5mA at 18V power supply voltage. The circuit is designed for 8-bit or 10-bit high resolution TFT LCD panels. The buffer has high slew rate, 0.5mA static current and 1kohm resistive and capacitive load driving capability. Also, it offers wide supply range, offset voltages below 50mV at 5mA constant output current, and below 2.5mV input referred offset voltage. To achieve wide-swing input and output dynamic range, current mirrored n-channel differential amplifier, p-channel differential amplifier, a class-AB push-pull output stage and an input level detector using hysteresis comparator are applied. The complete circuit is realized in a high voltage 0.18um 18V CMOS process technology for display driver IC and the area measures only 0.056mm^2. The circuit operates at supply voltages from 8V to 18V [21].

Soo-yang Park, Sang Hee Son, and Won Sup Chung (2005) a low-power rail-to-rail CMOS analog buffer is presented. The circuit is based on an input stage made up of two complementary class AB differential pairs, while a simple additional circuit allows rail-to-rail operation at the output terminal. The proposed circuit combines low static power consumption and high drive capability, resulting very suitable for applications with large capacitive loads. The buffer has been designed in a 0.35-μm CMOS technology to operate with a ±1.5 V dual supply. Simulated results are provided in order to demonstrate the proper operation of the proposed circuit. A rail-to-rail signal swing is achieved and a THD lower than –44 dB is obtained for a 2.4-Vpp 100-kHz input sinewave signal, whereas the input capacitance is lower than 32 fF [22].

Ali Far (2017) A CMOS subthreshold rail-to-rail input-output buffer amplifier suitable for energy harvesting applications is presented, having high gain (AV) of ~ 130dB, consuming ultra low currents (IDD) of ~ 150nA, and operating with low power supply voltage (VDD) > ~ 0.8v. Contributions of this work are the synthesis of the following attributes:
First, using a single transistor, the amplifier input stage's tail current is steered between the two PMOSFET input pairs, while one of the PMOSFET pairs is level shifted by a pair of NMOSFET source followers, which keeps the amplifier's input stage transconductance (gm) roughly constant while the inputs span rail-to-rail. Second, to boost folded cascade transconductance amplifier's (FCTA) AV, the proposed plurality of regulated cascode (RGC) current mirrors (CM) utilize a small size auxiliary amplifier, containing the same type and un-scaled FETs as that of the cascoded CMs employed within the FCTA. As such, the boosting of AV is less impeded by the otherwise higher impedance and high capacitance associated with scaled FETs, utilized in most prior art, in the RGC's auxiliary amplifier's signal path. Moreover, the RGC-CM utilizing the same FET, as that of the FCTA's CM, provides more consistency in FCTA's DC, AC, and dynamic response over process and operating condition variations.
Third, a buffer driver containing a Minimum Current Selector (MCS) and an inverting current mirror amplifier (ICMA) controls the quiescent current of the inactive output transistors (FETs), while a complementary noninverting current mirror (CNICM) curbs the current waste attributed to monitoring the FET's (external load) currents. The output buffer driver is inherently fast and can work at low VDD, since it operates mainly in current mode. Montecarlo (MC) and worst case (WC) simulations indicate the following specifications are achievable: input voltage range rail to rail; output voltage range ~ 10mV from the rails; resistive load (RL) 5K ohms capability; unity gain frequency (fu) ~ 200KHz and phase margin (PM) ~ 40 degrees; power supply rejection ratio (PSRR) ~ -90dB; common mode rejection ratio (CMRR) ~ -110dB; slew rate (SR) ~ 3V/ 10uS; settling time (ts) ~ 15uS; size ~130um/side [23].

Methodology	Advantages	Disadvantages
High Speed Buffer	1. High Input Impedance 2. Large output current	1. loss of bandwidth 2. Loss of voltage swing 3. Lower slew rate
CMOS analog Buffer	1. Extremely large fan-out capability (>50). 2. Lowest power dissipation of all gates (a few nW)	1. Increased cost due to additional processing steps. 2. Packing density less than NMOS.
Transconductance amplifier	1. It provides high output impedance. 2. High gain 3. High bandwidth	1. It consumes more power.
Differential Amplifier	1. Eliminate noise 2. Linear in nature	1. It rejects the common mode signal when operating
Operational Amplifier	1. Increased circuit stability. 2. Increased input impedance	1. Cannot be used for high frequencies. 2. Not suitable for working with medium and high powers

4. Conclusion

In this paper, we present the review of literature that shows the already work done in the field of rail-to-rail buffer amplifier in which various researchers uses different techniques for it such as differential amplifier, operation amplifier, CMOS amplifier, High-speed buffer etc. After study, we found that the above techniques is not completely efficient they have some disadvantages with advantages. So in future, we need to design such circuit or methodology, which can reduce the noise easily, and improve the performance and work in medium or high power.

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