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Evaluation and Designing of Efficient Multipoint FFT Algorithm

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Abstract: The Fast Fourier Transform is a most widely used for the application of the signal analysis and spectral analysis [1]. Usually in most of the Digital signal processing (DSP) based systems the Discrete Fourier Transform. has been used for the spectral analysis of signal The noise is usually randomly present in most of the DSP applications [2]. The spectral analysis based on the evaluating the performance of the Power spectral density (PSD) of the signal calculated suing the FFT of the signal plot. Also the amplitude spectral density is also defined using the FFT of the signal, this is the prime concern of this paper. The prime objective of this paper is to plan a proficient and fast FFT execution utilizing butterfly and folding technique. It needs to minimize the quantity of adders needed for FFT execution. It is additionally needed to execute and investigate the FFT for signal and unsigned values. FFT is actualized utilizing parameter like number of slice, number of LUTs, input output switch and maximum combinational path delay. The point of this work is to actualize a beneficial area and low concede 8-point, 16-point, 32-point, 64-point and 128-point obliteration as expected (DIT) and destruction in recurrence (DIF) FFT figuring for unsigned, stamped and complex number. We have also utilization radix-3 and radix-4 DIT and DIF computation for unsigned number.

Keywords: *DFT, Multipoint FFT, Radix-2, Decimation-In-Time, Decimation-In-Frequency, LUT, Folding Transformation, Feedback.*

I. INTRODUCTION

The Fast Fourier Transform is a most widely used for the application of the signal analysis and spectral analysis [1]. Usually in most of the Digital signal processing (DSP) based systems the Discrete Fourier Transform. has been used for the spectral analysis of signal The noise is usually randomly present in most of the DSP applications [2]. The spectral analysis based on the evaluating the performance of the Power spectral density (PSD) of the signal calculated suing the FFT of the signal plot. Also the amplitude spectral density is also defined using the FFT of the signal, this is the prime concern of this paper.

Figure 1.1 shows the execution of fast Fourier transform, that is partitioned into three classes. The genuine work actualized by researchers can be ordered in three unique classifications as

1) pipeline technique
2) parallel technique
3) pipeline and parallel technique.

Picture data, especially top quality picture is passing on huge proportion of data, nevertheless, the limit and planning of pictures for specific devices are under enormous weight [3]. A generous number of necessities for persistent transmission of intelligent media data in various correspondence systems are moreover a remarkable test much under the current high correspondence transmission rate. Thusly, capable picture pressure expects a vital part in such cases [4].

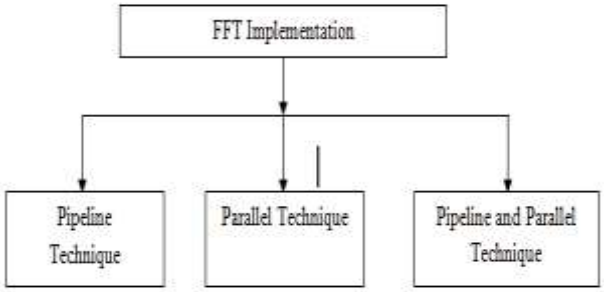

Fig 1: Classification of FFT Implementation.

Folding Transformation is a strategy where the amount of butterflies in a comparative segment is planned into one butterfly unit. In case we think about a FFT of size N, at that point 2-parallel designing can be gotten if we see the collapsing variable as N/2 or 4-parallel plan if considering a collapsing component of N/4. By choosing the appropriate collapsing sets we can determine the FFT structures [5][6]. The collapsing sets are formed in a way to deal with decline the amount of limit components and besides the lethargy. The previous FFT structures had no productive strategy for approach. This designing improves the blueprint of FFT and is a precise methodology towards the arrangement of FFT with optional degree of parallelism. These are determined either in Decimation-In-Time (DIT) or Decimation-In-Frequency (DIF) stream graphs. FFT constructions can be determined for different radices.

Figure 1.2 demonstrates the with collapsing technique are used. There are three same kinds of square are used for least deferral and immense region. In collapsing strategy are used to same piece taking all things together automated and picture dealing with [7].

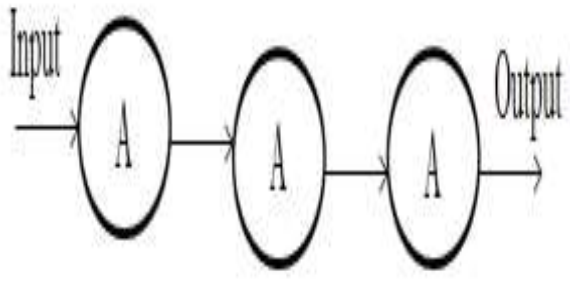

Fig.2: Folding Technique.

The rest of this paper is organized as follows. This paper is aimed to address the designing of efficient redix 8 FFT and evaluation of the various FFT methodologies. Then uses of FFT is explored for uunderstanding how the strength of a signal is distributed in the frequency domain, relative to the strengths of other ambient signals, the FFT is widely being used for evaluating the performance of the signal processing application in the presence of the noise.Section 1 gives describes the basic introduction to of the Fourier Transform, and the Fast Fourier Transform (FFT), Section 2 gives challenges in FFT design. Section 3 gives literature review and section 4 gives description about DFT. Section 5 introduces simulation tools and section6 gives proposed FFT algorithm. Comparative results are discussed in section 7. Section 8 concludes the paper.

2. CHALLENGES OF FFT DESIGN

Remembering the ultimate objective to meet the requests of current flag dealing with applications, multi-focus frameworks [1], [2] have ended up being amazingly common in the latest years. They can finish fast computations of a ton of data. This opens new possible results for bleeding edge computations in numerous fields. Regardless, the current example of growing the amount of focuses in like manner has many disadvantages.

An enormous number of planning units prompts to higher power usage and to a greater expense of the structure. Thus, it should be viewed as when multi-focus frameworks are really required and when we can indeed do the estimations in a lone contraption, provoking to save assets in imperativeness, money and trademark resources. With this point of view at the highest point of the priority list, this paper separates which is the computational power that can be typical these days on a singular field programmable entryway exhibit (FPGA). Thus, the paper concentrates the example of the speedy Fourier change (FFT), which is a champion among the most appropriate computations for flag getting ready. It is used as a piece of endless applications in a broad assortment of fields, from correspondence frameworks, to helpful applications and picture taking care of. Remembering the ultimate objective to do the examination, we have developed a gadget that produces high-throughput FFT utilization on FPGAs. The instrument thinks about masterminding various parameters, for instance, FFT measure, measure of parallelization, word length, radix, usage of BRAM memories, etc. By contrasting these parameters, the instrument produces FFT IP focuses with various execution limits.

3. RELATED WORK

This section surveys the different existing work partner to fast Fourier transform dependent on parallel architecture. In chapter likewise talked about the benefits and inconveniences of parallel and pipeline architecture utilizing image processing application. This segment audits the current work done in the field of the FFT. The entire writing audit is partitioned into three section for example audit of pipeline technique based FFT, survey of parallel technique based FFT and audit of parallel-pipeline based FFT.

Keshab K. Parhi et al. in [1] have introduced a low-complexity algorithm and architecture to register power spectral density (PSD) utilizing the Welch technique. The Welch algorithm gives a decent gauge of the spectral power at the expense of high computational complexity. We propose another changed way to deal with lessen the

computational complexity of the Welch PSD calculation for a half cover. In the proposed approach, an - point FFT is registered, where is the length of the window and is converged with the FFT of the past point to produce a point FFT of the covered segment. This requires supplanting the windowing activity as a convolution in the frequency domain.

F. Attivissimo et al. in [2] have proposed another strategy for spectral precise estimation of noisy signals; the significant disadvantage brought about by trade-off between spectral resolution and variance is inspected. The principle point of the paper is to show how the accuracy of periodogram estimation can be improved by embracing nonlinear averaging techniques of in part covered time slice of data sample .

Jameel Ahmad et al. in [3] have planned three FFT architecture that fall inside the Cooley-Tukey class of algorithm. These FFT plans are focused for OFDM applications particularly in people in the future of Software Defined Radio (SDR) frameworks. The FFT is performed on 64-point complex esteemed information samples with 16-cycle precision. Each center is enhanced for a blend of area, power, and speed.

Repala Akhil et al. in [4] have executed the 8-point Radix-2 DIT (Decimal In Time) FFT. In the FFT algorithm the fidget factor age by conventional technique for creating sine and cosine is traded by the CORDIC algorithm for mathematical functions. For the multiply and accumulate unit, various multipliers were utilized to be specific CORDIC multiplier, Single precision floating point multiplier. The adder blocks utilized in the usage are direct adders like Ripple Carry Adder (RCA) and parallel prefix adders like Kogge-Stone Adder (KSA).

Marwa Chafii et al. in [6] have concentrated analytically and experimentally the PSD of Wavelet-ODFM, and explicitly for the HAAR wavelet, since this last has been advanced in the writing for its few benefits, however its impediments have rarely been examined. We show that the bandwidth productivity of HAAR Wavelet-OFDM is more unfortunate than regular OFDM, having huge fundamental lobe and side lobes contrasted and OFDM.

Pramod Kumar Mehe e al. in [10] have examined a FFT processor of length 1024-point utilizing pipeline diagram. This arrangement used the normality of radix-22 FFT figuring. The use of FFT processor was acquired with just four measures of complex multipliers and a data memory of 1024 center interests. The chip had been perceived with 0.5 µm CMOS improvement with a district of 40 mm2 at a rehash of 30 MHz. To diminish the unconventionalities of premise, the sequential mode was gotten a handle on to subject the data into three tasks, for example, considered duplicating window, control of FFT and tally of module-square.

Naman Govil et al. in [15] have talked about that in the systems of OFDM, the match of FFT and IFFT am utilized for change and demodulation of data on the carriers of the baseband hail. The Verilog was used for coding the arrangement and a brief timeframe later stacked into Xilinx FPGA. The butterfly segment of this calculation and Radix 2 continue as in the past yet its assorted nature of duplication is same as that of Radix-4.

In the current years, the correspondence frameworks need to send voice and video indications of top quality in a compelling manner. In this manner there is a stunning fundamental for a speed powerful and solid advancement of correspondence. Orthogonal Frequency Division Multiplexing (OFDM) is a particularly solid other alternative to fulfill the above fundamental. Since the effect of semiconductor movements keep rising, the execution besides increments in parallel. Regardless, the utilization of force by processors in these rising movements additionally keeps expanding amazingly. The prime objective of this dissertation is to plan a proficient and fast FFT execution utilizing butterfly and folding technique. It needs to minimize the quantity of adders needed for FFT execution. It is additionally needed to execute and investigate the FFT for signal and unsigned values. FFT is actualized utilizing parameter like number of slice, number of LUTs, input output switch and maximum combinational path delay. The point of this work is to actualize a beneficial area and low concede 8-point, 16-point, 32-point, 64-point and 128-point obliteration as expected (DIT) and destruction in recurrence (DIF) FFT figuring for unsigned, stamped and complex number. We have also utilization radix-3 and radix-4 DIT and DIF computation for unsigned number.

4. DISCRETE FOURIER TRANSFORM

Transforms such as discrete Fourier transform (DFT) are a major block in many communication systems like OFDM, etc. DFT is likewise considered as one of the significant devices to perform recurrence investigation of discrete time signals. A discrete time succession can be spoken to by tests of its range in the recurrence area, utilizing DFT. The Discrete Fourier Transform is a consistent Fourier change for the instance of discrete capacities. Graphically the operation can be view using FFT flow graph shown in Figure 5. From this figure, the FFT computation is accomplished in three stages.

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The discrete Fourier transform (DFT)

$$X(k)=\sum_{n=0}^{N-1}x(n)W_N^{kn}, \qquad k=0,1,\ldots,N-1$$

Where $W_N=e^{-j(2\pi/N)}$. The inverse discrete Fourier transform (IDFT) is

$$x(n)=\frac{1}{N}\sum_{k=0}^{N-1}X(k)W_N^{-kn}, \quad n=0,1,\ldots,N-1$$

Fig 3: The Formulation of the DFT calculation

For the complex case of the input sequence X(n)

$$X(k)=\sum_{n=0}^{N-1}\{(\mathrm{Re}[x(n)]\mathrm{Re}[W_N^{kn}]-\mathrm{Im}[x(n)]\mathrm{Im}[W_N^{kn}]) + j(\mathrm{Re}[x(n)]\mathrm{Im}[W_N^{kn}]+\mathrm{Im}[x(n)]\mathrm{Re}[W_n^{kn}])\},$$

$$k=0,1,\ldots,N-1$$

Fig4: the DFT formulation in case if the complex input.

The foundation of flag and picture preparing involves different quantities of calculations of FFT. By and large the calculations are assessed in view of the quantity of duplications and increments. This work brings up that different variables, for example, multifaceted nature and consistency are likewise required for the effective execution of a FFT processor notwithstanding the above element.

The usage of basic type of outlines incorporate less number of endeavors and little blunders when contrasted with normal type of plans. Consequently these basic outlines diminish the advertising time and their plan time can be utilized for mimicking the key outline parameters. The standard sorts of blueprints are all things considered worked by the basic building squares and they fuse tinier number of parts. Regardless, these arrangements acknowledge bigger piece of the favorable circumstances accomplished by that of clear diagrams.

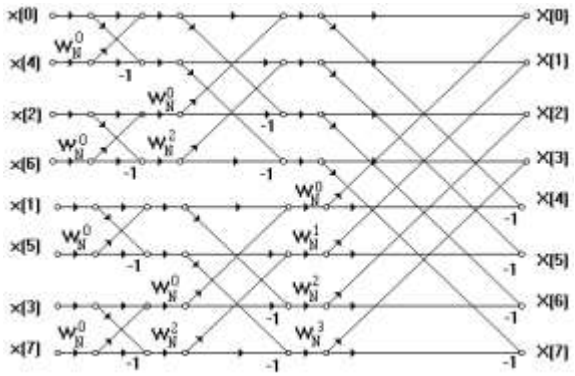

Fig 5: FFT Signal Flow Graph

The DFG can be pipelined is shown in Figure 6 to ensure that folded hardware has non-negative number of delays. The folded delays for the pipelined DFG are

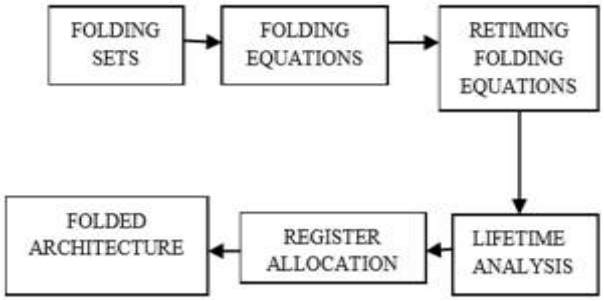

Fig 6: Block diagram of FFT design techniques

5. SIMULATION TOOL

Condition setup is the workplace or devices on which result investigation has been accomplished for Xilinx 6.2i. Xilinx is the extremely solid programming instrument to examination and reproduce the mind boggling circuits. There are such a variety of variants for Xilinx programming, for example, 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. For the most part two programming dialect are utilizing VHDL and Verilog.

VHDL is an acronym for VHSIC equipment depiction dialect (VHSIC is an acronym for fast incorporated circuits). It is an equipment depiction dialect that can be utilized to show an advanced framework at many levels of ingestion going from the calculation level to the entryway level [14]. VHDL permits clients or software engineers to utilize certain pieces which involve certain arrangement of successive proclamations. One such square is known as a procedure. The (<=) administrator, it is known as the task administrator and is utilized just to assign qualities to signals. For factors the administrator utilized is (:=).

Some main terms that are utilized at the fundamental level are: - Libraries, Data sorts, Signals, Variables, Entity, and Architecture. Other critical terms for the VHDL program, for example, prepare, part, capacity, methods and state graphs are utilized as a part of programming.

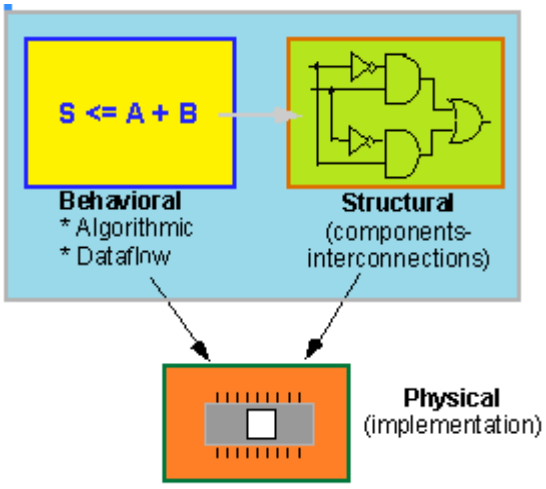

Fig 7: basic design methodologies for VHDL

6. PROPOSED FFT ALGORITHM

According to base paper, the use different technique used for decimation in time (DIT) and decimation in frequency fast Fourier transform (FFT) using pipeline and parallel technique. In base paper generally concentrate on the number of slice (area), number of look up table (LUT) and maximum combination path delay (MCPD) of the fast Fourier transform. In this dissertation proposed folding technique based DIT FFT using array multiplier, signed multiplier and complex multiplier. So step by step explain proposed design is given below, flowchart is shown in figure 8 and block diagram is shown in figure 9.

(1) Design serial in serial out shift register using delay flip flop.

(2) For design sign multiplier using AND gate for generate partial product and these partial product added by half adder, full adder. We can also design proposed complex multiplier with the help of three multipliers.

(3) By the help of half and full adder and sub-tractor design N-bit adder and N-bit sub-tractor.

(4) Design single path delay feedback pipeline structure.

(5) Same block are used to different level we have design to folding technique.

(6) All step are included we have design fast Fourier transform.

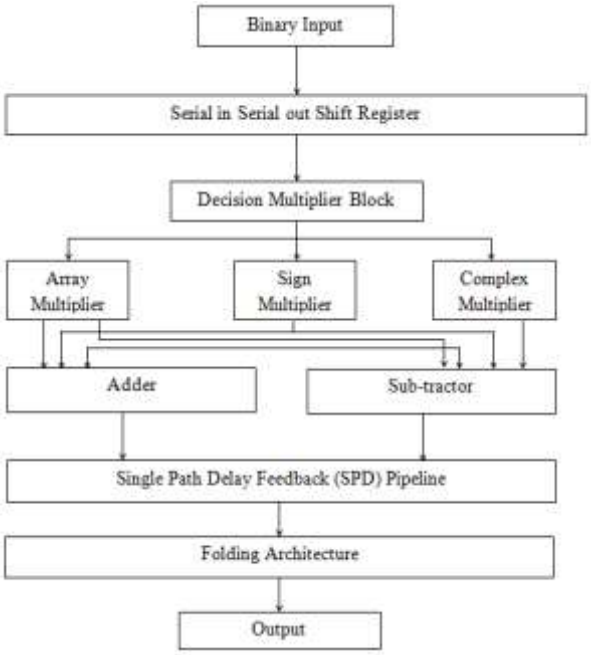

Fig 8: Flow Chart of the Proposed FFT Architecture

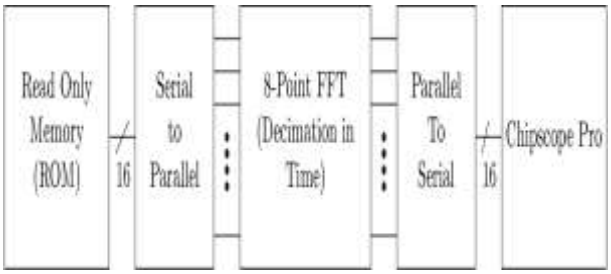

Fig 9: The block diagram implementation of the proposed N point FFT

7. COMPARATIVE RESULTANALYSIS

Comparative results of using multiplier add operation (T_{MA}), add multiplier operation (T_{AM}), radix-2 DIT FFT algorithm using eight point, sixteen point, thirty two point, sixty four point and one hundred twenty eight point in terms of area occupied (Number of Slices), delay involved (Maximum Combinational Path Delay), LUT has been shown in Table 7.2-7.4 respectively.

In Table 7.2 shown the results of multiplier adds operation and add multiplier operation that can be implemented in the Xilinx 6.2i. We have designed all coding using Very High Scale Integrated Circuit Hardware Description Language (HDL). To get minimum delay compared to existing algorithm.

Table 1: Computational Delay of 8 bit Mult-add And Add-Mult Operations

Architecture	T_{MA}	T_{AM}	T_{AM-} T_{MA}	% Difference
Base paper Design	8.345	8.967	0.622	6.9%
Proposed Design	8.048	8.653	0.295	3.5%

Table 2: Computational Delay of 16 bit Mult-add And Add-Mult Operations

Architecture	T_{MA}	T_{AM}	T_{AM-} T_{MA}	% Difference
Base paper Design	9.453	10.321	0.868	8.4%
Proposed Design	8.653	9.240	0.587	6.3%

Table 7.3: Computational Delay of 32 bit Mult-add And Add-Mult Operations

Architecture	T_{MA}	T_{AM}	T_{AM-} T_{MA}	% Difference
Base paper Design	14.532	14.982	0.45	3.0%
Proposed Design	13.377	14.010	0.633	4.5%

Comparative results of using multiplier add operation (T_{MA}), add multiplier operation (T_{AM}), radix-2 DIT FFT algorithm using eight point, sixteen point, thirty two point, sixty four point and one hundred twenty eight point in terms of area occupied (Number of Slices), delay involved (Maximum Combinational Path Delay), LUT has been shown in Table 1,2 and 3respectively.

These tables shown the results of multiplier adds operation and add multiplier operation that can be implemented in the Xilinx 6.2i. We have designed all coding using Very High Scale Integrated Circuit Hardware Description Language (HDL). To get minimum delay compared to existing algorithm.

We have also shown the bar graph of the 8-point 16-point and 32-point multiplier add operation and add multiplier operation in Figure 4.30, Figure 4.31 and Figure 4.32 respectively.

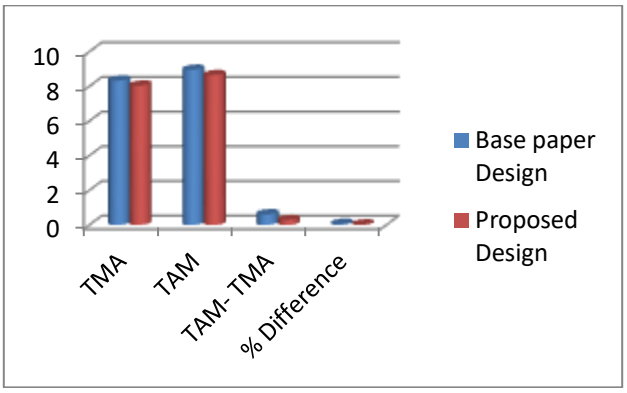

Fig10 : Bar Graph of the Existing and Proposed Mult-Add and Add-Mult Butterfly for N=8.

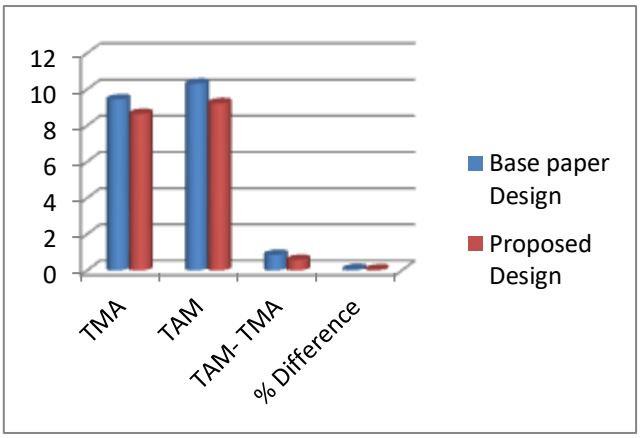

Fig 11: Bar Graph of the Existing and Proposed Mult-Add and Add-Mult Butterfly for N=16.

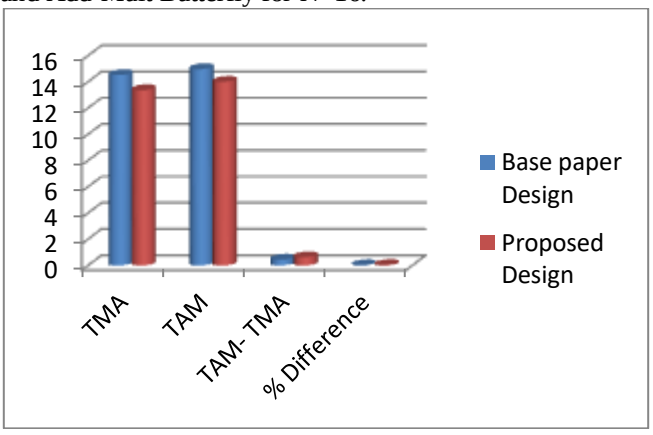

Fig 12 : Bar Graph of the Existing and Proposed Mult-Add and Add-Mult Butterfly for N=32.

8. CONCLUSION

By studying how the strength of a signal is conveyed in the frequency domain, comparative with the qualities of other ambient signals, the FFT is generally being utilized for assessing the performance of the signal processing application within the sight of the noise. Our work has also utilized radix-3 and radix-4 DIT and DIF computation for unsigned number. This work is the combination of the implementations of array multiplier, signed multiplier and complex multiplier. Design of this proposed work has increased 7.6% in the speed of radix-2 unsigned DIT FFT algorithm and also increased 10.4% in the speed of radix-2 signed DIT FFT algorithm. Our design radix-2 DIT FFT algorithm using folding technique has utilized value of design parameters such as LUTs, number of slice and MCPD. Radix-2 DIT FFT algorithm using folding technique is also used for complex multiplier by utilizing the optimum value of design parameter such as LUTs, slice and MCPD. The results of the input signal and the noisy signals used for the PSD evaluation is at the sample frequency of 500 Hz and the results of the PSD evaluation is at the selected input line sample frequency of the 50 Hz.

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